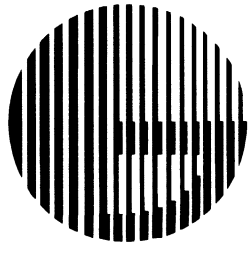
GENNUM
CORPORATION



designers and manufacturers of integrated circuit products with full inhouse capabilities for CAD/CAM, silicon process, testing, packaging and applications assistance.

1990 – 1991
IC DATA BOOK

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Excellence Through People and Technology!

CONTENTS

Section 3 continued

Section 4 - Analog ASICs & IC Array Products data sheets

Section 5 - Hearing Instrument Products shortform listing

ALPHABETICAL AND NUMERICAL LISTING OF GENNUM PRODUCTS

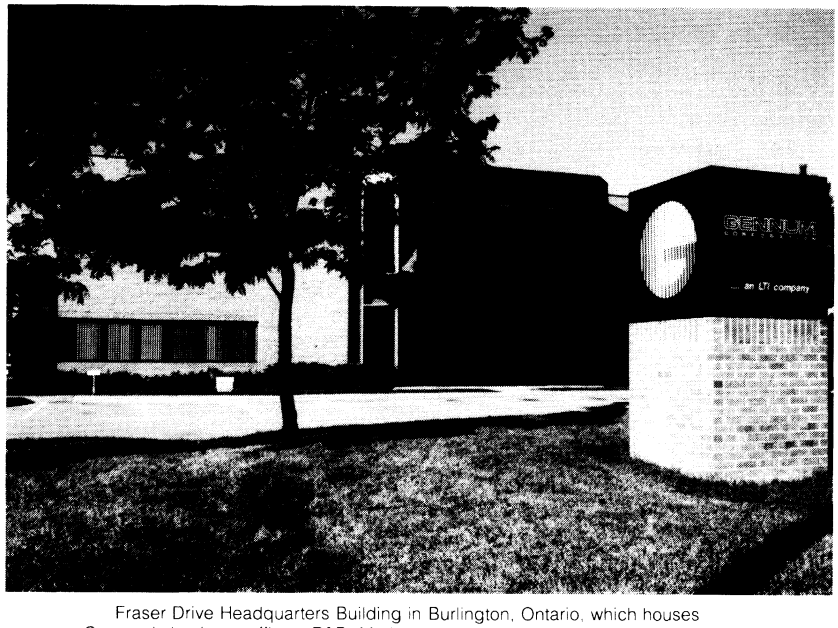
AND DEVICE ORDER NUMBERS

DEVICE NO.	PAGE NO.	DESCRIPTION		ORDER NO.	DOCUMENT NO.
GM8108	2-47	8x1 HDTV Mux.	32 pin SIP	GM8108 - CSG	510-93
GM8110		10x1 HDTV Mux.	40 pin SIP	GM8110 - CSH	
GM8116	2-49	16x1 Mux.	45 pin SOIC wide	GM8116 - CSK	510-76
GM8216		16x1 Mux.	45 pin SOIC narrow	GM8216 - CSK	
GM8316		16x1 CCTV Mux.	45 pin SOIC wide	GM8316 - CSK	
GM8416		16x1 CCTV Mux.	45 pin SOIC narrow	GM8416 - CSK	
GP2842	3-29	Current Mode PWM Controller	16 pin DIP	GP2842 - ID -	510-11
GP6040	3-9	Single-ended RM Controller	16 pin DIP	GP6040 - CDC	510-59
			16 pin SOIC	GP6040 - CKC	
GP6041	3-9	Single-ended RM Controller	16 pin DIP	GP6041 - CDC	510-59
			16 pin SOIC	GP6041 - CKC	
GP605	3-1	RM Power Supply Controller	16 pin DIP	GP605 - - CDC	510-43
			16 pin SOIC	GP605 - - CKC	
			16 pin DIP	GP605 - - IDC	
			16 pin SOIC	GP605 - - IKC	
GP6050	3-17	Push-pull RM Controller	16 pin DIP	GP6050 - CDC	510-58
			16 pin SOIC	GP6050 - CKC	
GP6051			16 pin DIP	GP6051 - CDC	510-58
			16 pin SOIC	GP6051 - CKC	
GP6140	3-21	ZVS Single-ended RM Contr.	16 pin DIP	GP6140 - CDC	510-97
			16 pin SOIC	GP6140 - CKC	
			16 pin DIP	GP6140 - EDC	
			16 pin SOIC	GP6140 - EKC	
			16 pin SOIC	GP6140 - MDC	
GP6141	3-21	ZVS Single-ended RM Contr.	16 pin DIP	GP6141 - CDC	510-97
			16 pin SOIC	GP6141 - CKC	
			16 pin DIP	GP6141 - EDC	
			16 pin SOIC	GP6141 - EKC	
			16 pin SOIC	GP6141 - MDC	
GX214	2-37	4x1 Crosspoint Switch	14 pin DIP	GX214 - - CDB	510-55
			14 pin SOIC	GX214 - - CKB	
			16 pin SOIC	GX214 - - CKC	
GX401	2-1	1x1 Crosspoint Switch	chip	GX401 - - CC -	510-9-3
			7 pin SIP	GX401 - - CSN	
GX411	2-5	1x1 Crosspoint Switch, dual latch	8 pin SIP	GX411 - - CSA	510-56
GX414	2-23	4x1 Crosspoint Switch	chip	GX414 - - CC -	510-38
			14 pin DIP	GX414 - - CDB	
			16 pin SOIC	GX414 - - CKC	
GX414A	2-33	4x1 Crosspoint Switch	14 pin DIP	GX414 - ACDB	510-19
			16 pin SOIC	GX414 - ACKC	

DEVICE NO.	PAGE NO.	DESCRIPTION		ORDER NO.	DOCUMENT NO.
GX4201	2-9	4x1 Wideband Xpt Sw.(Tally)	8 pin DIP 8 pin SOIC	GX4201 - CDA GX4201 - CKA	510-74
GX424	2-23	4x1 Crosspoint Switch	14 pin DIP 16 pin SOIC	GX424 - - CDB GX424 - - CKC	510-38
GX4301	2-15	1x1 Wideband Crosspoint Sw.	8 pin SOIC 8 pin SIP	GX4301 - CKA GX4301 - CSA	510-94
GX4304	2-41	4x1 Wideband Crosspoint Sw.	14 pin DIP 14 pin SOIC 16 pin SOIC	GX4304 - CDB GX4304 - CKB GX4304 - CKC	510-91
GX4314	2-41	4x1 Wideband Crosspoint Sw.	14 pin DIP 14 pin SOIC 16 pin SOIC	GX4314 - CDB GX4314 - CKB GX4314 - CKC	510-91
GX4324	2-41	4x1 Wideband Crosspoint Sw.	14 pin DIP 14 pin SOIC 16 pin SOIC	GX4324 - CDB GX4324 - CKB GX4324 - CKC	510-91
GX4334	2-41	4x1 Wideband Crosspoint Sw.	14 pin DIP 14 pin SOIC 16 pin SOIC	GX4334 - CDB GX4334 - CKB GX4334 - CKC	510-91
GX434	2-23	4x1 Crosspoint Switch	14pin DIP 16 pin SOIC	GX434 - - CDB GX434 - - CKC	510-38
GX4404	2-45	4x1 Wideband Xpt Sw. (Tally)	16 pin DIP 16 pin SOIC	GX4404 - CDC GX4404 - CKD	510-90
GX4414	2-45	4x1 Wideband Xpt Sw. (Tally)	16 pin DIP 16 pin SOIC	GX4414 - CDC GX4414 - CKD	510-90
GY4102	2-19	Fast Toggling Crosspoint Sw.	8 pin DIP 8 pin SOIC	GY4102 - CDA GY4102 - CKA	510-40

All above devices order (part) no.s must consist of a combination of 10 components, (letters, numbers or spaces).
See also page 1-16.

LD405	3-27	RM Power Supply Controller	16 pin DIP 16 pin SOIC	LD405D LD405K	510-4
		For replacement parts only			



Fraser Drive Headquarters Building in Burlington, Ontario, which houses Gennum's business offices, R&D, Marketing, Masking, Test and Assembly areas.

The Landmark Road facility, also in Burlington, Ontario, where all the silicon processes are located.

Gennum Corporation supplies electronic components to manufacturers of electronic systems all over the world. Our business is the design, manufacture and marketing of silicon integrated circuits, (ICs). Employing over 200 people, Gennum is housed in two modern facilities in Burlington, Ontario, just a few miles west of Toronto. A recent addition is the opening of an office in Tokyo, Japan. To better serve our worldwide customers Gennum has 31 agents and/or design centres in 14 countries.

Gennum Corporation, created in 1987, continues the integrated circuit operations, conducted since 1973, by LTI, Gennum's parent company. This business which Gennum Corporation continues has grown to more than seventeen million dollars of sales in 1989, sharing in the tremendous growth which has been experienced in electronic component manufacturing since 1973.

Gennum's continued growth has occurred because of a business philosophy: - attention to individuals' needs; customers, suppliers, employees and investors alike.

Capabilities in terms of human and physical resources extend through all facets of the company. These include technology development, new product design and development, and all aspects of wafer fabrication, device assembly and testing. Skills and abilities are constantly improved through the application of the latest tools and technologies applied to new products and existing products alike. This gives Gennum customers the competitive advantage essential to their success.

Currently Gennum Corporation serves five distinct areas within the electronic systems and subsystems market.

- resonant mode controller ICs for power supplies.
- crosspoint switches for the video/broadcast industry
- special application products
- semicustom IC linear arrays
- low voltage, low current hearing instrument products such as amplifiers and filters.

This comprehensive catalog provides detailed information on products in all five areas, with data sheets, application notes, and packaging information. Applications assistance is available at any time from our applications engineers.

Corporate Mission:

Excellence Through People and Technology!

- serve the customer
- respect people
- pursue excellence

The exacting processes of integrated circuit design and production force a hard discipline on those who manufacture them and Gennum Corporation is no exception to this rule.

The company's silicon processing includes linear bipolar circuits with operating ranges from as low as 1.0V up to 30V, transistor current handling capability up to 3A, and 2.5 GHz f_T transistors. In combination with the above, ion implanted JFETs and Schottky diodes can be added. A recent addition to our capablities is CMOS technology.

To help us stay in the forefront of technology, Gennum maintains affiliations with the scientific and engineering departments of five Canadian universities.

Computer aided design is a major component of our product development cycle. The highly efficient equipment and personnel are able to shorten design time and cost while increasing reliability. Simulation programs such as SPICE, SUPREM and COMPACT are available in-house for design optimization. Their use allows investigation of circuit performance under the most extreme cases of device matching and over as wide a range of temperature as necessary.

To ensure that every product meets Gennum's high quality standards, we perform in-line sample inspection on each batch from incoming inspection, to the final test of the finished product. Gennum's entire manufacturing process is governed by strict production controls performed by production personnel, as well as quality control audit inspections to double check the quality practices instituted by other groups.

1. Order Acceptance

No order is contractually binding on Gennum Corporation unless accepted in writing by an authorized representative of the Company. All orders are accepted in accordance with the terms outlined herein notwithstanding any conflicting terms which may appear on the Buyer's order.

Orders will be accepted for:

1.1 Complete delivery in a single shipment on a specific date. These are called Single Shipment Orders.

1.2 Delivery in many shipments spread over an extended period. These are called Extended Period Blanket (EPB) Orders.

2. Contractual Period

2.1 A purchase order which has been accepted in accordance with Paragraph 1 above, will be contractually binding on both Seller and Buyer for the contractual period, which lasts from the date of first shipment to the date on which the total quantity of units ordered has been shipped by the Seller or for twelve months, whichever comes first.

2.2 The contractual period may be extended beyond the twelve month limit provided both Buyer and Seller agree so to do in writing.

3. Prices

Prices shown on a quotation will remain firm for the validity period of the quotation. Prices shown on an order acknowlegement will remain firm during the contractual period, except that a price decrease which is freely offered by the Seller will apply to all shipments made after its effective date.

4. Termination of an Order

An order shall be automatically terminated at the end of the contractual period. The Buyer may terminate an order prematurely by providing the Seller with 60 days notice in writing. In the event of premature termination the following shall apply.

4.1 The Seller is entitled to ship all parts which were previously scheduled for shipment before termination date by the Buyer.

and

4.2 The Buyer is liable for payment for all parts shipped in accordance with Paragraph 4.1 above, including additional payments arising from increased per unit prices at the reduced quantity. The Buyer is liable for back billing for all parts shipped at the applicable blanket order prices.

and

4.3 Payment of a reasonable charge based upon expenses incurred and commitments made in the execution of the purchase contract by Gennum Corporation up to the date of receipt of the notice of termination; the charge being a minimum of 15% of the unrealized invoice value of the order.

5. Extended Period Blanket (EPB) Orders

5.1 EPB Orders will be accepted for any products in quantities to cover expected requirements over the contractual period. The total of all products ordered may be used to determine the per unit price of each proprietary product accordance with the quotation submitted by the Seller to the Buyer.

5.2 Changes to EPB orders by the Buyer, including changes in device types ordered, and changes in order quantity, either decrease or increase, will be accepted by the Seller subject to the following limitations:

5.2.1 Within 3 months from date of order acceptance, a change in total quantity ordered, either an increase or decrease, which results in the total number of units being in a different price/quantity range, will automatically change the per unit price for all prior and subsequent shipments.

5.2.2 At any time after order acceptance, changes in device types ordered, either by addition, deletion, or substitution, shall at the discretion of the Seller, require sixty days notice in writing.

6. Shipping Schedule

Unless purchase orders are accompanied by a shipping schedule, shipment will be at the Seller's discretion. In the case of Extended Period Blanket Orders, the order must be accompanied by a shipping schedule which releases at least 40% of the total order quantity for shipment in a period not to exceed five months from the beginning of the contractual period. The remaining parts on a EPB order may be released at the Buyer's discretion provided:

6.1 All parts are scheduled for **shipment** within the Contractual Period.

and

6.2 The Buyer provides the Seller with at least 12 weeks notice of any new shipping requirement or amendment to existing shipping schedule.

7. Terms of Payment

The terms of payment agreed between the Seller and Buyer will be clearly shown on the Order Acceptance document supplied by the Seller to the Buyer. Until credit terms have been negotiated, the only terms of payment which will be accepted by the Seller are cash with order. Gennum Corporation reserves the right to apply a monthly service charge not in excess of two percent per month, on the overdue payment balance, provided it supplies the Buyer with thirty days notice in writing.

8. Loss or Damage in Transit or Short Shipment

All shipments should be inspected by the Buyer immediately upon receipt. If there is evidence of loss or damage during transit, the Buyer should immediately file a claim with the carrier. Gennum Corporation will cooperate with the Buyer to ensure that a proper adjustment with the carrier is obtained. In the event of short shipment, claims must be made directly to Gennum Corporation in writing within fifteen working days after receipt of goods.

9. Warranty

Gennum Corporation warrants that its products will be free of defects in material and workmanship and will perform as specified in the governing data sheet for one year from date of shipment. The liability of Gennum Corporation is limited to repairing, replacing F.O.B. Burlington, Ontario, Canada, products which are returned by the Purchaser at **his expense** during the warranty period. Final determination as to whether a product is actually defective rests with Gennum Corporation. This warranty shall automatically become null and void if the products are used in an unreasonable manner or in a manner which exceeds the absolute maximum ratings specified by the governing data sheet.

9.1 Returns - Warranty

An RMO number and authorization must be obtained from Gennum Corporation before material is returned.

9.1.1 If an entire shipment is being returned based on a Quality Assurance Sampling Process, the defective devices must first be sent to Gennum Corporation for confirmation. Once confirmed, the entire shipment may be returned, following normal procedures. Devices which have been used or subjected to any production process are not eligible for credit.

9.2 Non-Warranty

Any product returned for reasons other than defective must receive an RMO number and authorization and will be subject to a restocking charge.

10. Limitation of Liability

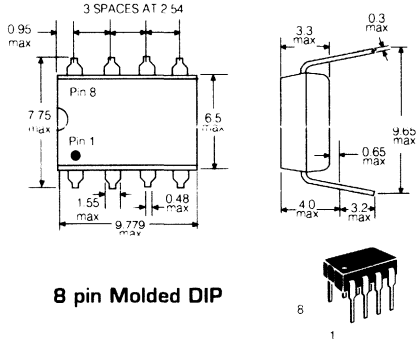
Notwithstanding any other provision in this contract or any applicable statutory provisions, neither Gennum Corporation nor the purchaser shall be liable to the other for special or consequential damages or damages for loss of use arising directly or indirectly from any breach of this contract (fundamental or otherwise) or from any tortius acts or omissions of their respective employees or agents and in no event shall the liability of Gennum Corporation exceed the unit price of the product.

11. Force Majeure

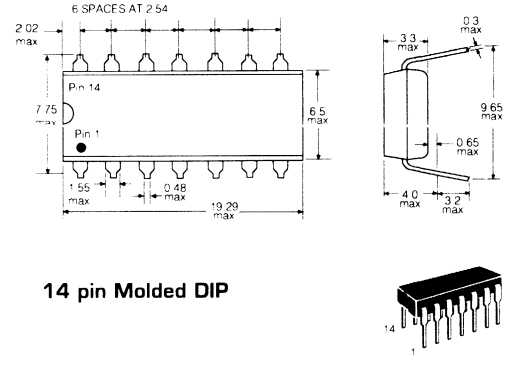
Gennum Corporation shall not be responsible or liable for any loss, damage, detention or delay caused by war, invasion, insurrection riot, the order of any civil or military authority, or by fire, flood, weather or other acts of the elements, breakdown, lockouts, strikes or labour disputes, the failure of its suppliers to meet their contractual obligations, or, without limitation of the foregoing, any other cause beyond its reasonable control and the receiving of the product by the Purchaser shall constitute a waiver of all claims for loss or damage due to delay.

AVAILABLE PACKAGING & PART NUMBERING (see page 1-16)

Gennum can provide a wide variety of proprietary and standard packages.

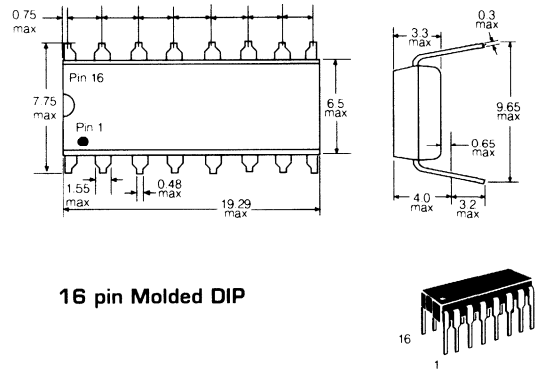


8 pin Molded DIP



14 pin Molded DIP

Other standard DIP packaging is available for custom and semicustom products.



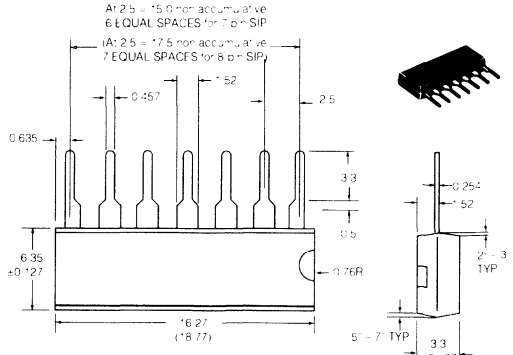
16 pin Molded DIP

DIP PACKAGES

All dimensions in millimetres

OTHER STANDARD PACKAGING

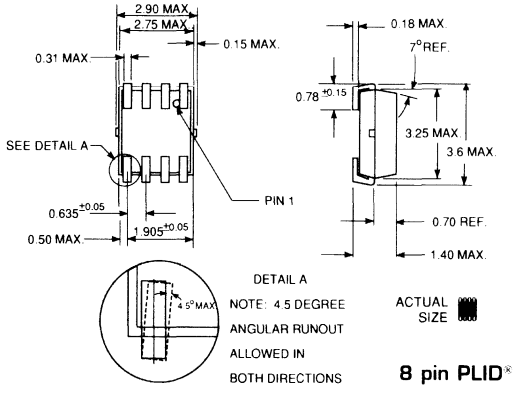
All dimensions in millimetres



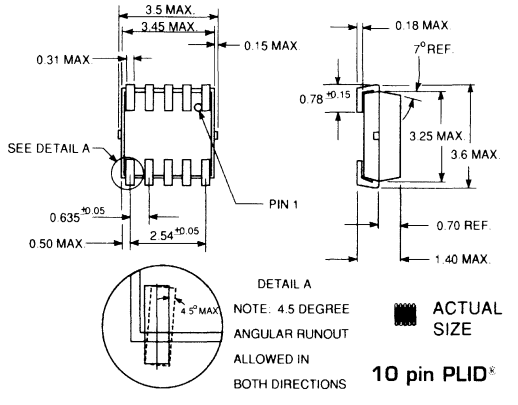
7 and 8 pin SIP

GENNUM PROPRIETARY PACKAGING

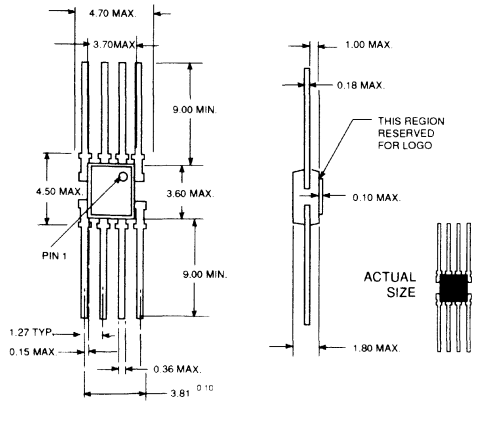
All dimensions in millimetres



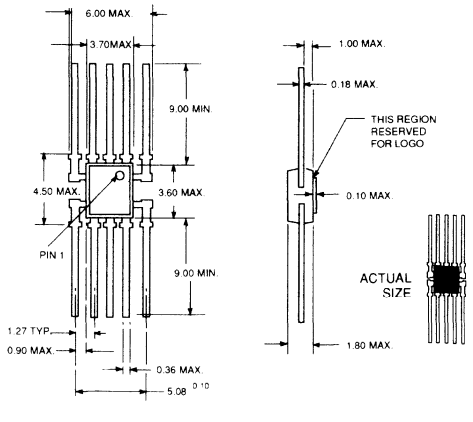
8 pin PLID®



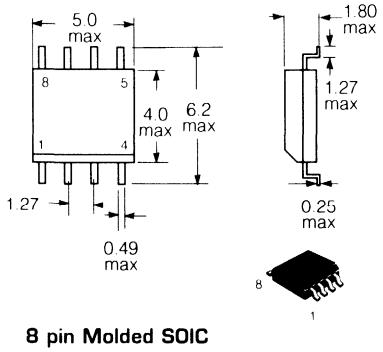
10 pin PLID®



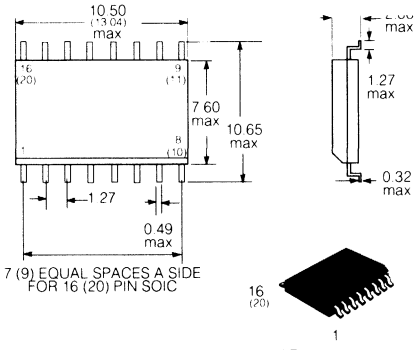
8 pin MINIpac



10 pin MINIpac



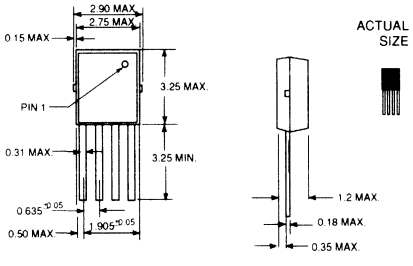
8 pin Molded SOIC



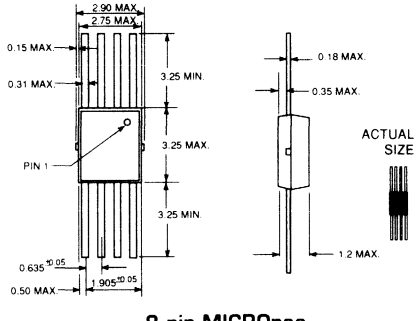
16 and 20 pin Molded SOIC

GENNUM PROPRIETARY PACKAGING **continued**

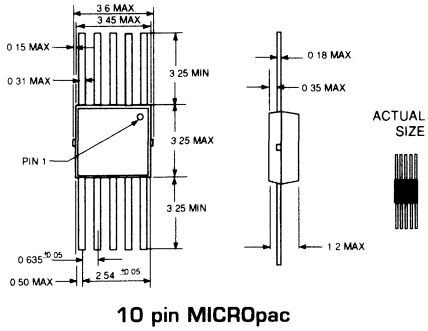
All dimensions in millimetres



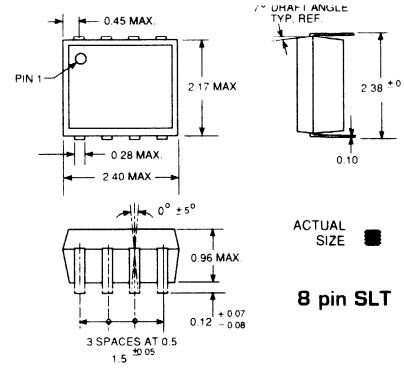
4 pin MICROpac



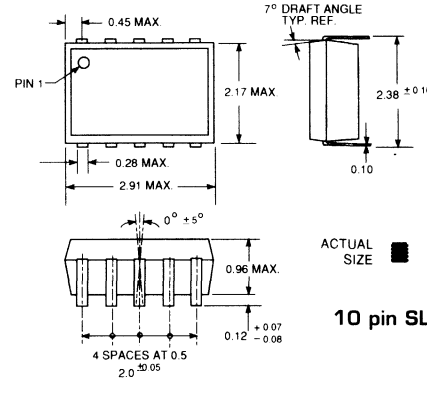
8 pin MICROpac



10 pin MICROpac



8 pin SLT



10 pin SLT

GENNUM PROPRIETARY PRODUCTS PART NUMBERING SYSTEM

Description/Family

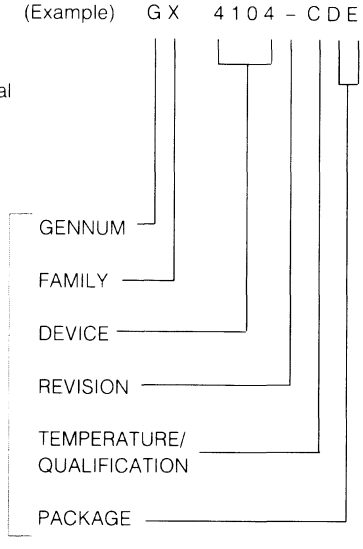
G – GENNUM

A – Array
B – Buffer
C – Amplifier
F – Filter
I – Interface
K – Custom
M – Modules
O – Oscillators
P – Power
T – Transconductance

Temperature/Qualification

C – Commercial
E – Extended Industrial
I – Industrial
M – Military

The part number must consist of a combination of 10 components, (letters, numbers or spaces).



PACKAGES

CC **Chip**

DA	8 0.3	**plastic**	**DIP**
DB	14 0.3	"	"
DC	16 0.3	"	"
DE	18 0.3	"	"
DF	20 0.3	"	"
DG	22 0.4	"	"
DH	24 0.3	"	"
DI	24 0.6	"	"
DJ	28 0.3	"	"
DK	28 0.6	"	"
DL	40 0.6	"	"

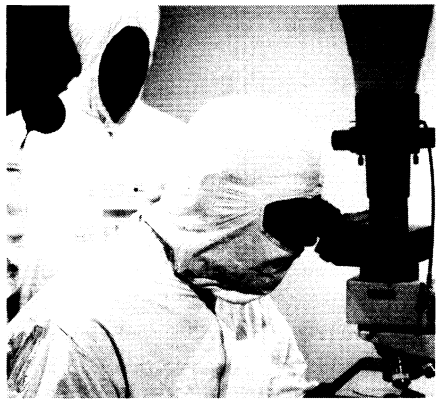
EA	8 0.3	**ceramic**	**DIP**
EB	14 0.3	"	"
EC	16 0.3	"	"
EE	18 0.3	"	"
EF	22 0.4	"	"

KA	8 0.15	**SOIC**
KB	14 0.15	"
KC	16 0.3	"
KD	18 0.15	"
KF	22 0.4	"

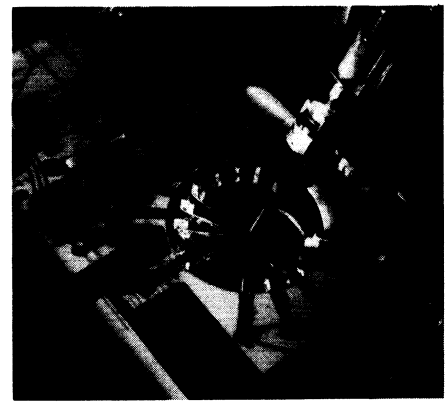
PJ	28	**PLCC**
PM	44	"

SA	8 0.3	**SIP**	
SF	20	"	
SG	32	"	**MODULES**
SH	40	"	"
SK	45	"	"
SN	7 0.3	"	

For product order number designations see pages 1-6 and 1-7



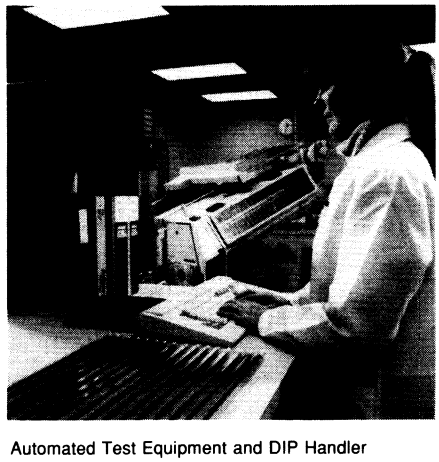
Wafer Inspection



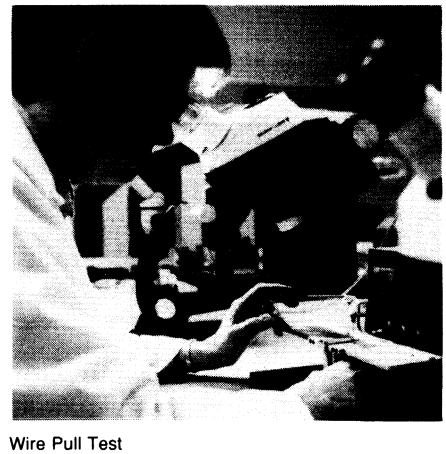
Automated Wafer Probe

RELIABILITY THROUGH QUALITY

- **Procedures designed to meet MIL.STD.105D**
- **Quality audits**
- **All employees participate in the "Quality Improvement Process"**
- **Products are sampled for reliability at all stages of manufacture.**



Automated Test Equipment and DIP Handler



Wire Pull Test

QUALITY IMPROVEMENT JOURNEY

Quality is important in any industry but even more so in a high-tech environment. Companies such as Gennum, that market on a global scale must pursue quality relentlessly.

This commitment to quality commenced in earnest in the mid 1980's with intensive quality tralning for all Gennum employees. The quality focus is on employee participation and interaction. Therefore you'll find quality circles, or teams, or task forces operating in design, marketing, manufacturing, administration, human resources and building services. Performance indicators and goals are defined and monitored constantly, and variances are analyzed. The precepts of quality are threefold:

In all activities

- *know the job requirements,*
- *set standards to meet requirements,*
- *conform to standards.*

Gennum's quality improvement results are known and respected by our customers, more than half of whom do not perform any incoming inspection of our products. Our average outgoing quality (AOQ) defects level has been halved in each of the last six years, a visible result of a quality program that works. Our vision of quality effectiveness is achieving a goal of zero defects.

Gennum's products are sold in 20 countries on five continents. With this wide customer base and a broad spectrum of products, customer satisfaction is of vital importance. It has been said that quality means — measure, measure, and measure. This is especially true for measurement of customer satisfaction. Since the late 1980's this has been incorporated in the business plans of the marketing groups. We are proud that our customer's rating of their satisfaction with Gennum is consistantly above industry average.

THE PEOPLE

Gennum employees are the cornerstone of our quality processes. As part of the quality training, employees learn that:
knowlege + practice + feedback = success.
This is an integral part of the quality process at Gennum and is followed by the application of that training in all aspects of the job. Finally the measurement feedback assures that quality is an ongoing improvement journey.

At Gennum the emphasis is on prevention of error, rather than the analysis of failure. With this in mind, Gennum's Quality Assurance department fulfills the function of auditing the quality of processes, products, systems and procedures, at the same time endeavouring to instill in each employee an awareness to be their own quality control inspector. Of course Q.C. stations do exist throughout the production and design areas, however, the ultimate responsibility rests with each employee within each process. Prevention of error is, of course, much more cost-effective than appraisal. Therefore the Quality Assurance group is only a final "gate" in the path to customer satisfaction.

THE TOOLS

Gennum's philosophy states that each employee is responsible for quality and quality improvement. Therefore, tools for day-to-day work activities are an important resource to attain quality and excellence. These range from powerful networked PC's and work-stations, to state-of-the-art computer aided design (CAD) facilities. The administrative data processing runs a full "MRP II" program with capabilities to attain class A operation.

In the last five years Gennum has spent an average of 5% per annum of revenue to increase,upgrade and operate its computational, design and operational hardware and software.

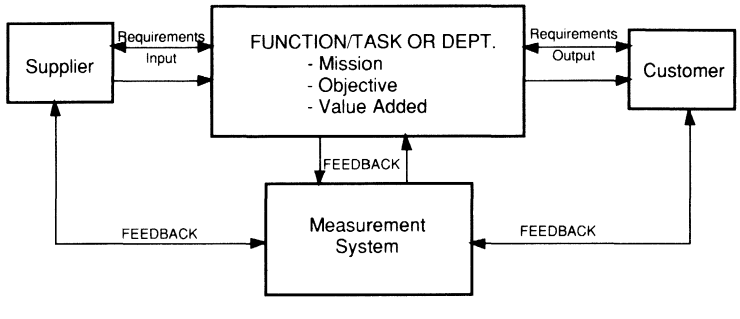
Gennum's Quality Assurance group has a wide range of specialized and precision hardware. This ranges from automatic test equipment (ATE) for electrical tests , to scanning electron microscopes for visual analysis. Process and product qualifications use sophisticated reliability and failure analysis equipment.

WORLD CLASS EXCELLENCE

Gennum's benchmarks for excellence are the industry norms. Traditionally industry standards were set by the Japanese. However, with the introduction in 1988 of the Malcolm Baldridge National Quality Award in the U.S.A., a new vigour has developed in the West. This ensures that standards improve yet remain competitive.

The judging critieria for the Malcolm Baldrige National Quality Awards are sevenfold and summarize Gennum's focus and efforts:

1. LEADERSHIP
   It measures the success of senior management in creating and sustaining a quality culture.
2. INFORMATION AND ANALYSIS
   This measures the effectiveness of the company's collection and analysis of information for quality planning and improvement.
3. PLANNING
   Planning judges the effectiveness of integration of quality requirements into the company's business plans.
4. HUMAN RESOURCE UTILIZATION
   It measures the success of the company's efforts to utilize the full potential of the workforce for quality.
5. QUALITY ASSURANCE
   QA looks at the effectiveness of the company's systems for assuring quality control of all operations.
6. QA RESULTS
   QA evaluates the company's results in quality achievement and quality improvement, demonstrated through quantative measures.
7. CUSTOMER SATISFACTION
   It judges the effectiveness of the company's systems to determine customer requirements and demonstrated success in meeting those requirements.



IMPROVING THE QUALITY OF PROCESS

QUALIFICATION

The purpose of qualification is to ensure that only reliable products will be introduced into the manufacturing stage, and ultimately reach the marketplace.

Two levels of qualification test routines are performed on all new product designs at Gennum.

1. Initial Qualification from
   Design to Preproduction

   - representative sample
   - attribute tests
   - high temperature storage
   - temperature shocks
   - attribute tests
   - report

2. Follow-up Qualification from
   Preproduction to Production

   - representative sample
   - attribute tests
   - high temperature burn-in
   - temperature cycle
   - attribute tests
   - pressure cook/temperature
     humidity bias (95°C / 95%RH)
   - attribute tests
   - report

CALIBRATION

A calibration program has been established which covers all equipment used to design, manufacture, test and inspect products. This program is traceable to national standards and is performed inhouse by an independent service from outside the company.

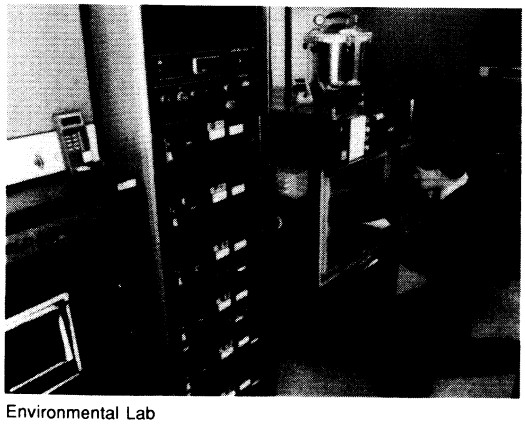
QUALITY LEVELS

Quality means conformance to defined specifications and standards, through measureable and monitable parameters. MIL.STD.38510 is used for general specifications of microelectronics.

At the output of Wafer Fabrications, and Assembly Operations, Quality Assurance gates have been established to ensure that in-line systems are effectively producing products which conform to specifications. Guidelines for Gennum quality inspection is MIL.STD.883C for test methods and procedures for microelectonics, and BR513, a 70 page Die Inspection Criteria document using method 2010, class B.

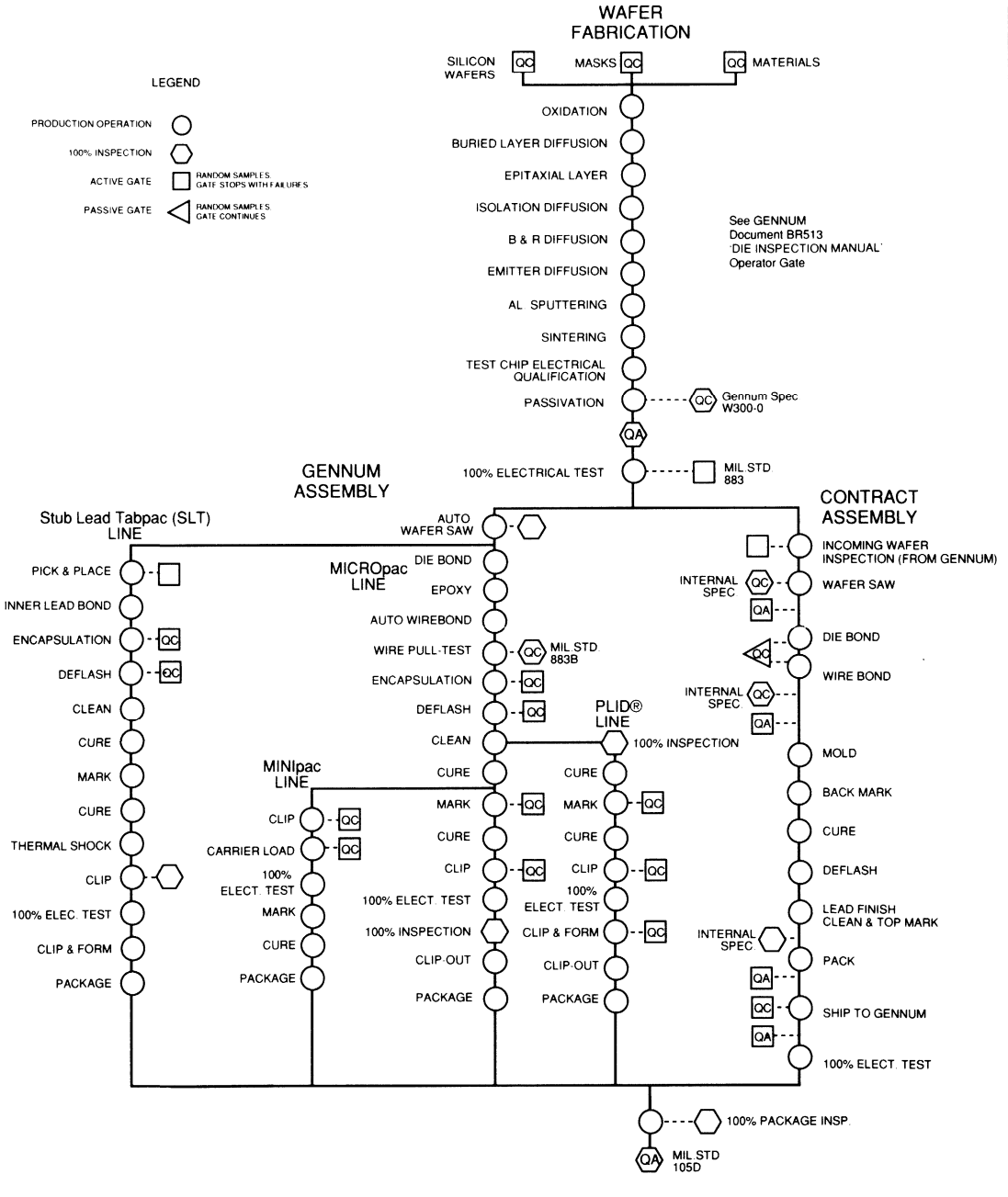
All finished devices are subject to both mechanical and electrical inspection based in MIL.STD.105D sampling plans. All outgoing inspection data is analyzed so as to monitor outgoing quality performance.

The Ultimate Goal: Zero Defects



Environmental Lab

Q.A. Station



QUALITY PROCEDURES FLOW CHART

VIDEO & BROADCAST PRODUCTS

GENNUM CORPORATION

Monolithic 1x1 Video Crosspoint Switch

GX401 DATA SHEET

FEATURES

- 100 MHz bandwidth (-3 dB)
- insertion loss 0.03dB at 100 kHz
- gain spread ±0.075dB at 8 MHz
- differential gain at 3.58 MHz 0.04% (max)
- differential phase at 3.58 MHz 0.02° (max)
- TTL and 5 V CMOS compatible logic inputs
- compatible with all popular video standards
- 7 pin single-in-line package
- built-in enable latch allows synchronous selection

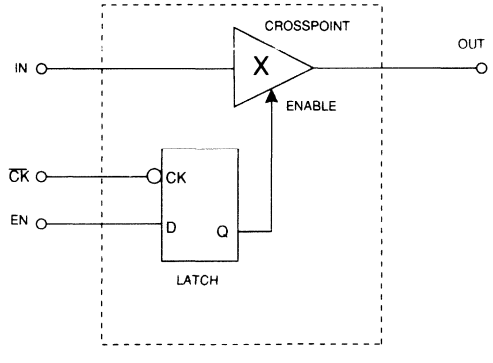
CIRCUIT DESCRIPTION

The GX401 is a low cost monolithic 1x1 video crosspoint switch plus on-board latch, designed primarily for use in video switching applications where 1 out of N channel selection function is required. Unlike similar devices using MOS bilateral switching elements, the GX401 represents a fully buffered unilateral transmission path when enabled, and offers better than 90 dB of off-isolation at 10 MHz when disabled.

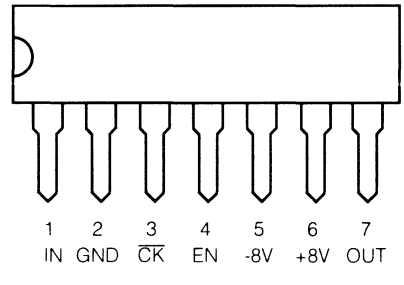
In addition, the GX401 offers wide bandwidth and superior differential gain and phase performance.

Power supply requirements are ±8 volts. Logic inputs are TTL and 5V CMOS compatible.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Parameter	Value
Supply Voltage	±10.0 V
Operating Temperature Range	0° C ≤ T_A ≤ 70° C
Storage Temperature Range	-65° C ≤ T_S ≤ 150° C
Lead Temperature (Soldering, 10 Sec)	260° C
Analog Input Voltage	-4 V ≤ V_{IN} ≤ 2.4 V
Logic Input Voltage	-4 V ≤ V_L ≤ 5.25 V

NOTE: Output is not short circuit protected.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range
GX401 - - CSN	7 Pin SIP	0° to 70°C

GENNUM CORPORATION P.O. Box 489, Stn A, Burlington, Ontario, Canada L7R 3Y3 tel. (416) 632-2996 fax: (416) 632-2055 telex: 061-8525
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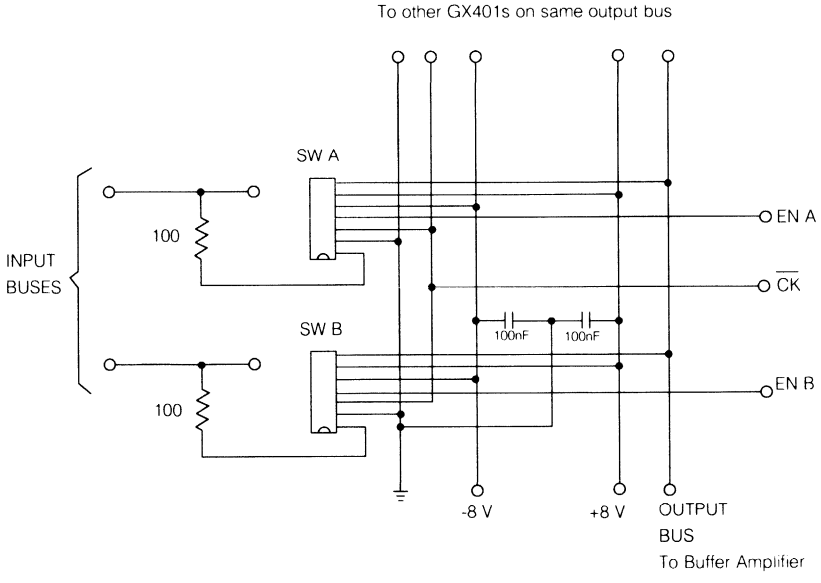
ELECTRICAL CHARACTERISTICS (V_S = ±8V DC, 0°C < T_A < 70°C, R_L = 10kΩ, C_L = 30pF. Typical values are at T_A=25°C)

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC SUPPLY	Supply Voltage	V_S ±		7.5	8.0	8.5	V
	Supply Current	I+	Chip selected (EN=1)	-	15	18	mA
			Chip not selected (EN=0)	-	0.7	0.9	mA
		I-	Chip selected (EN=1)	-	14	17	mA
			Chip not selected (EN=0)	-	0.63	0.85	mA
STATIC	Analog Output Voltage Swing	V_{OUT}	Extremes before clipping occurs	-1.2	-	+2.0	V
	Output Offset Voltage	V_{OS}	75Ω resistor on each input to gnd	5	15	25	mV
	Output Offset Voltage Drift-	$\Delta V_{OS} / \Delta T$		-	50	200	µV/°C
LOGIC	Crosspoint Turn-On Time	t_{ON}	Control input to appearance of signal at output.	300	400	500	ns
	Crosspoint Turn-Off Time	t_{OFF}	Control input to disappearance of signal at output.	900	1200	1600	ns
	Clock input Pulse width	t_{CK}	Control input to appearance of signal at output.	350	-	-	ns
	Logic Input	V_{IH}	1	2.0	-	-	V
	Thresholds	V_{IL}	0	-	-	0.8	V
	Enable	$I_{BIAS(EN)}$	EN = 1	-	-	2.0	µA
	Bias Current		EN = 0	-	-	-0.1	µA
DYNAMIC	Insertion Loss	I.L.	1V p-p sine or sq. wave at 100 kHz	0.02	0.03	0.05	dB
	Bandwidth (-3dB)	B.W.		100	-	-	MHz
	Gain Spread at 8 MHz			-	-	±0.075	dB
	Input Resistance	R_{IN}	Chip selected (EN = 1)	900	-	-	kΩ
	Input Capacitance	C_{IN}	Chip selected (EN = 1)	-	2.0	-	pF
			Chip not selected (EN = 0)	-	2.2	-	pF
	Output Resistance	R_{OUT}	Chip selected (EN = 1)	-	12	-	Ω
	Output Capacitance	C_{OUT}	Chip not selected (EN = 0)	-	7	-	pF
	Differential Gain	dg	f = 3.58 or 4.43 MHz	-	0.03	0.04	%
	Differential Phase	dp	V_{IN} = 40 IRE	-	0.01	0.02	degrees
	Off Isolation		Crosspoint on output to gnd. f = 10 MHz	90	-	-	dB

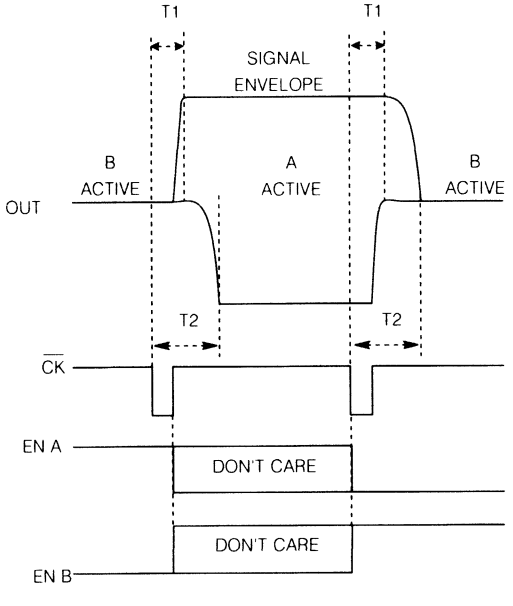
AVAILABLE PACKAGING

7 pin SIP

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION



TYPICAL GX401 APPLICATION CIRCUIT



CONDITIONS:
Input B: grounded via 75Ω
Input A: 1V p-p sinewave
T1 = 400 ns
T2 = 1.2 µs

NOTE:
Clock is level triggered

TYPICAL CROSSPOINT SELECTION TIMING DIAGRAM

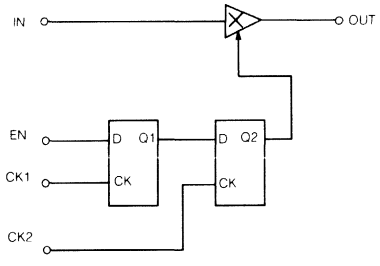
Monolithic 1x1 Video Crosspoint Switch with Two Latches

GX411 PRELIMINARY DATA SHEET

FEATURES

* differential gain at 3.58 MHz, 0.05% (max.)
* differential phase at 3.58 MHz, 0.025 deg.(max.)
* dual latches
* off-isolation at 10 MHz, 90 dB (min.)
* -3 dB bandwidth, 100 MHz (min.)
* insertion loss at 100 kHz, 0.03 dB (typ.)

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLES

EN	CK1	CK2	Q1	Q2
0	1	0	0	$Q2_{n-1}$
0	1	1	0	0
1	1	0	1	$Q2_{n-1}$
1	1	1	1	1
X	0	0	$Q1_{n-1}$	$Q2_{n-1}$
X	0	1	$Q1_{n-1}$	$Q1_{n-1}$

X = DON'T CARE

Q2	OUT
0	HIGH Z
1	IN

ORDERING INFORMATION

Part Number	Package	Temperature Range
GX411 - - CSA	8 pin SIP	0°C to 70°C

CIRCUIT DESCRIPTION

The GX411 is a broadcast quality 1x1 video crosspoint featuring two control latches, implemented in bipolar monolithic technology. The device is characterized by low differential gain and phase, extremely high off isolation, and a -3 dB bandwidth of 100 MHz.

For use in NxM routing matrices, the GX411 features very high output impedance in the disabled state. This allows multiple devices to be paralleled at the input and output without additional circuitry. A fully buffered unilateral signal path ensures negligible output to input feedback while delivering minimal output switching transients through make-before-break switching.

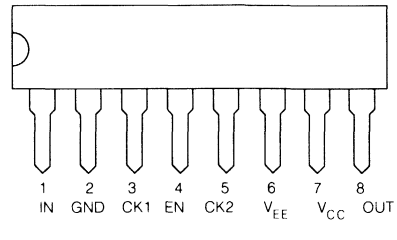
To maximize system bandwidth, an external current source is used to bias the output device of the crosspoint. One external current source is required per output bus. For less demanding applications, a load resistor can be used in place of the output current source, causing a slight increase in differential phase. Non-additive mixing will occur on the output bus if more than one paralleled GX411 is enabled at a time.

Dual transparent latches allow asynchronous addressing and synchronous switching. The control microprocessor can write to the input latch using *CK1*, while the video timing clock can be used to initiate switching using *CK2*. Alternatively, one or both of the latches can be made transparent by pulling *CK1* or *CK2* high.

The device operates over a supply voltage range from ±7 to ±13.2 volts. With a supply voltage of ±8 V, the device dissipates only 8 mW in the disabled state.

APPLICATIONS

- video routing switchers
- video production and master control switchers
- CCTV / CATV



PIN CONNECTION
8 PIN SIP

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JAPAN BRANCH: 301 Aoba Building, 3-6-2 Takanawa, Minato-ku, Tokyo 108, Japan tel. (03) 441-2096 fax: (03) 448-8991

ABSOLUTE MAXIMUM RATINGS

Parameter	Value
Supply Voltage	±13.5 V
Operating Temperature Range	0 °C ≤ T_A ≤ 70 °C
Storage Temperature Range	-65 °C ≤ T_S ≤ 150 °C

Parameter	Value
Lead Temperature (Soldering, 10 Sec)	260 °C
Analog Input Voltage	-5 V ≤ V_{IN} ≤ V_{CC}+0.3 V or V_{EE} +20 V
Logic Input Voltage	0 V ≤ V_L ≤ 5.5 V

ELECTRICAL CHARACTERISTICS (V_S = ±8 V DC, 0°C < T_A < 70 °C, R_L = 10 kΩ, C_L = 30pF, I_L = 2 mA)

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC SUPPLY	Supply Voltage	$\pm V_S$		7	8	13.2	V
	Supply Current (I_L of 2 mA not included)	I+	Q2 = 1	-	9.7	12.6	mA
			Q2 = 0	-	0.45	0.59	mA
		I-	Q2 = 1	-	9.5	12.4	mA
			Q2 = 0	-	0.38	0.5	mA
STATIC	Analog Output Voltage Swing	V_{OUT}	Extremes before clipping occurs	-2	-	5.5	V
	Analog Input Bias Current	I_{BIAS}		-	20	-	µA
	Output Offset Voltage	V_{OS}	T_A = 25 °C	-10	-	10	mV
	O/P Offset Voltage Drift	$\Delta V_{OS} / \Delta T$		-	50	200	µV / °C
LOGIC	Crosspoint selection Turn-on time	t_{ON}	From CK2	-	0.7	-	µs
			From EN	-	0.8	-	
	Crosspoint selection Turn-off time	t_{OFF}	From CK2	-	2.2	-	µs
			From EN	-	2.4	-	
	Clock Pulse Width	t_{CK}		500	-	-	ns
	Logic Input Thresholds	V_{IH}	1	2.0	-	-	V
		V_{IL}	0	-	-	1.1	V
	Enable Input Bias Current	$I_{BIAS(EN)}$	EN=1	-	0.5	3.0	µA
	CK1/CK2 Bias Current	$I_{BIAS(CK)}$	CK1/CK2=0	-	0.7	5.0	µA
DYNAMIC	Insertion Loss	I.L.	1V p-p sine or sq. wave at 100 kHz	0.02	0.03	0.05	dB
	Bandwidth (-3dB)	B.W.		100	-	-	MHz
	Gain Spread at 8 MHz			-	-	±0.06	dB
	Input Resistance	R_{IN}	Chip selected	1	-	-	MΩ
	Input Capacitance	C_{IN}		-	2	-	pF
	Output Resistance	R_{OUT}		-	15	-	Ω
	Output Capacitance	C_{OUT}		-	3.5	-	pF
	Differential Gain	dg	at 3.58 MHz V_{IN} = 40 IRE	-	-	0.05	%
	Differential Phase	dp		-	-	0.025	deg.
	Off Isolation		Crosspoint on output to gnd f = 10 MHz	90	100	-	dB
	Slew Rate	+SR	V_{IN} = 3V p-p (C_L = 0 pF)	120	190	-	V/µs
		-SR		110	170	-	

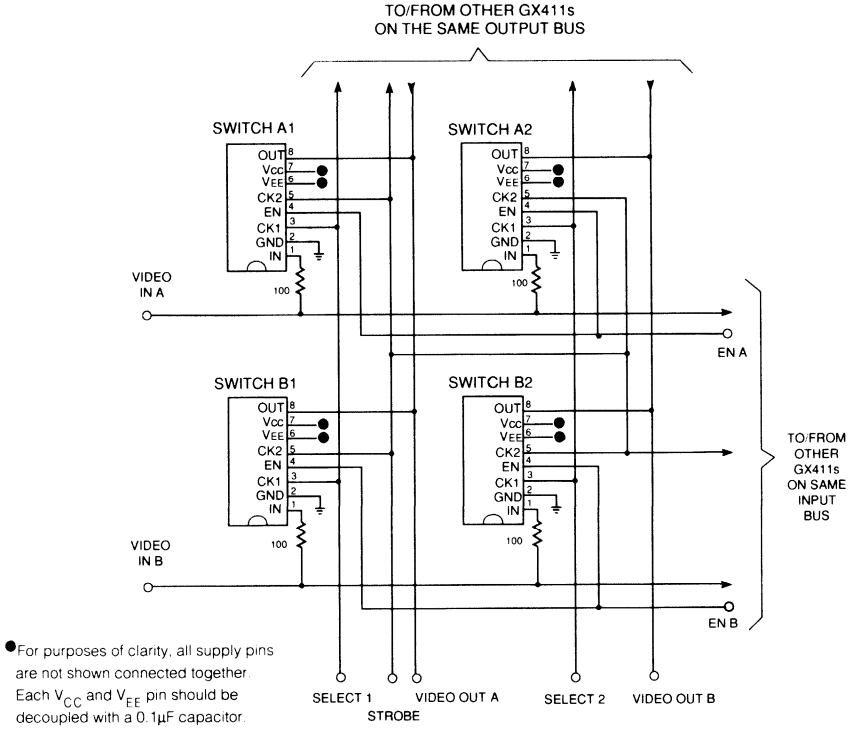


Fig 1 Typical Application Circuit of Four GX411's Connected as a 2x2 Matrix.

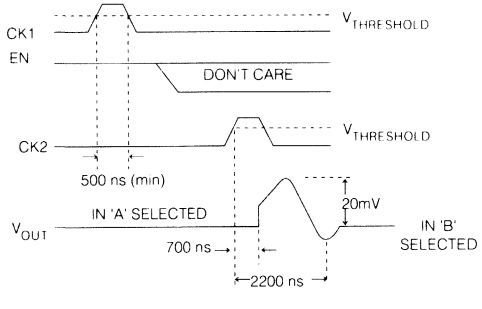


Fig. 2 Typical Crosspoint Timing Diagram

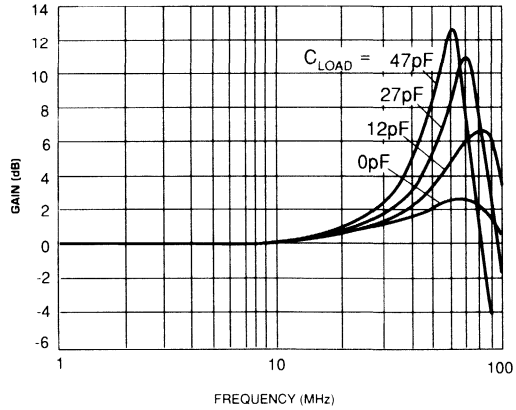


Fig. 3 Gain vs Frequency

CAUTION

ELECTROSTATIC SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE DEVICES EXCEPT AT A STATIC-FREE WORKSTATION

GENNUM CORPORATION

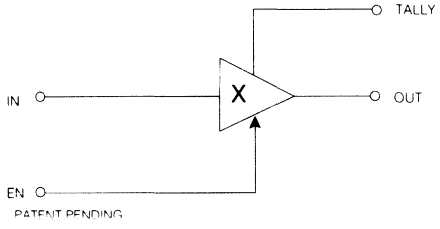
Wideband, Monolithic 1x1 Video Crosspoint Switch

GX4201 PRELIMINARY DATA SHEET

FEATURES

* -3 dB bandwidth, 300 MHz with C_L = 0 pF
* off isolation at 100 MHz, 80 dB
* differential phase and gain at 4.43 MHz, 0.01° & 0.02%
* 600 µW disabled power consumption
* input signal levels from -2 V to +3 V
* logic input compatible with TTL and 5 V CMOS
* open collector TALLY output

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

EN	OUT	TALLY
0	HIGH Z	OFF
1	IN	ON

ABSOLUTE MAXIMUM RATINGS

Parameter	Value
Supply Voltage	±7.5 V
Operating Temperature Range	0° C ≤ T_A ≤ 70° C
Storage Temperature Range	-65° C ≤ T_S ≤ 150° C
Lead Temperature (Soldering, 10 Sec)	260° C
Analog Input Voltage	-5.5 V ≤ V_{IN} ≤ 5.5 V
Logic Input Voltage	-0.5 V ≤ V_L ≤ 5.5 V
Output Load Current	12mA
High Level TALLY Output Current	2 mA

CIRCUIT DESCRIPTION

The GX4201 is a wideband 1x1 video crosspoint implemented in bipolar monolithic technology. The device is characterized by excellent differential gain and phase in the enabled state, and very high off-isolation in the disabled state. The fully buffered unilateral signal path ensures negligible output to input feedback while delivering minimal output switching transients through make-before-break switching.

For use in NxM routing matrices, the device features a very high, nearly constant input impedance, coupled with very high output impedance in the disabled state. This allows multiple GX4201's to be paralleled at the input and output without additional circuitry. An open collector PNP toV_{CC} TALLY output provides indication of crosspoint selection.

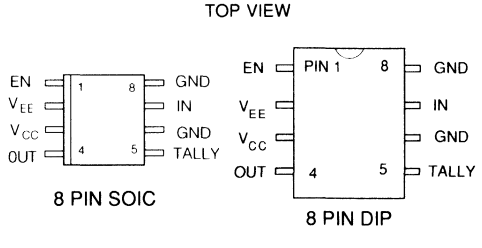
To maximize system bandwidth, an external current source is used to bias the output device of the crosspoint. One external current source is required per output bus. For less demanding applications, a load resistor can be used in place of the output current source, causing a slight increase in differential phase. Non-additive mixing will occur on the output bus if more than one paralleled GX4201 is enabled at a time.

The GX4201 is one of a series of wideband video crosspoints utilizing Gennum's proprietary LSI process.

APPLICATIONS

* very high quality video switching
* HDTV
* computer graphics
* RF switching/routing
* PCM/data routing

PIN CONNECTIONS



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ELECTRICAL CHARACTERISTICS (V_S = ±5V DC, 0°C < T_A < 70°C, I_L = 6 mA)

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
	Supply Voltage	$\pm V_S$		±4.5	±5	±5.5	V
DC		I+	EN=1	-	12	15.6	mA
SUPPLY	Supply Current		EN=0	-	50	100	µA
	(not including external	I-	EN=1	-	11	14.3	mA
	current load)		EN=0	-	70	140	µA
	Analog Output Voltage Swing	V_{OUT}	Extremes before clipping occurs	-2	-	3	V
STATIC	Analog Input Bias Current	I_{BIAS}		-	12	-	µA
	Output Offset Voltage	V_{OS}	T_A = 25°C	-10	-	10	mV
	Output Offset Voltage Drift-	$\Delta V_{OS} / \Delta T$		-	-25	-80	µV/°C
	Crosspoint Turn-On Time	t_{ON}	Control input to appearance of signal at output.	-	200	400	ns
LOGIC	Crosspoint Turn-Off Time	t_{OFF}	Control input to disappearance of signal at output.	0.5	1.0	-	µs
	Logic Input	V_{IH}	1	2.0	-	-	V
	Thresholds	V_{IL}	0	-	-	0.8	V
	Enable Bias Current	$I_{BIAS(EN)}$	EN = 0	-	-	2	µA
	TALLY Output	V_{OH}	EN = 1, I_O = 1mA	4.80	4.89	4.92	V
	Insertion Loss	I.L.	1V p-p sine or sq. wave at 100 kHz R_L=10K, C_L=30pF	-	0.025	-	dB
	Bandwidth (-3dB) See Fig. 1	B.W.	small signal C_L = 0 pF	-	300	-	MHz
	Input Resistance	R_{IN}	EN = 1	1.0	3.0	-	MΩ
DYNAMIC	Input Capacitance	C_{IN}	EN = 0	-	1.1	-	pF
	Output Resistance	R_{OUT}	EN = 1	-	7	-	Ω
	Output Capacitance See Fig. 5	C_{OUT}	EN = 0	-	1.1	-	pF
	Differential Gain	dg	at 3.58 MHz	-	-	0.04	%
	Differential Phase See Fig. 6	dp	V_{IN} = 40 IRE	-	-	0.04	degrees
	Off Isolation See Fig. 4		Enabled GX4201 on output f = 100 MHz V_{IN} = 1V p-p	-	80	-	dB
	Slew Rate	+SR		250	400	-	
		-SR	V_{IN} = 3V p-p (C_L = 0 pF)	250	350	-	V/µs

ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	TEMPERATURE RANGE
GX4201 - CKA	8 PIN SOIC	0° to 70°C
GX4201 - CDA	8 PIN DIP	0° to 70°C

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

TYPICAL PERFORMANCE CURVES OF THE GX4201

For all graphs, V_S = ±5 V DC and T_A = 25°C. The curves shown below represent typical batch sampled results.

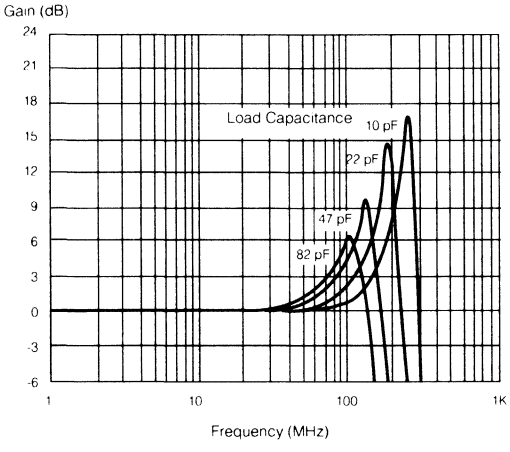


Fig. 1 Gain vs Frequency

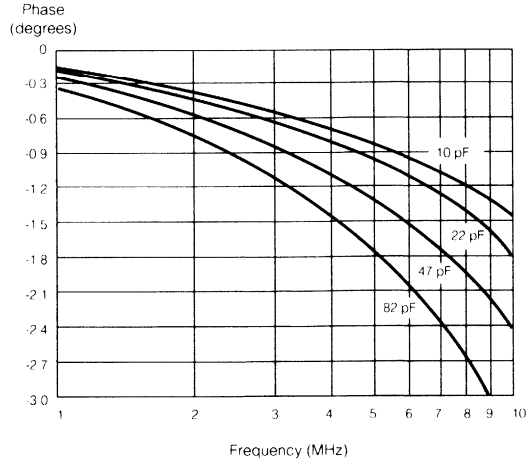


Fig. 2 Phase vs Frequency

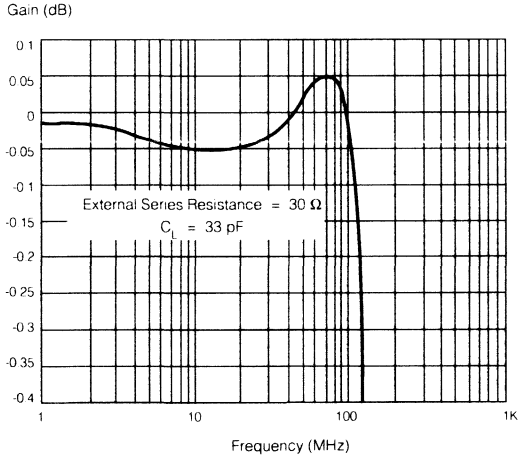


Fig. 3 Gain vs Frequency

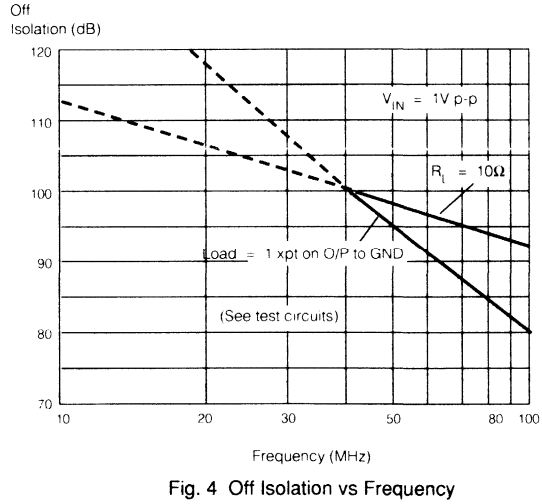


Fig. 4 Off Isolation vs Frequency

continued over

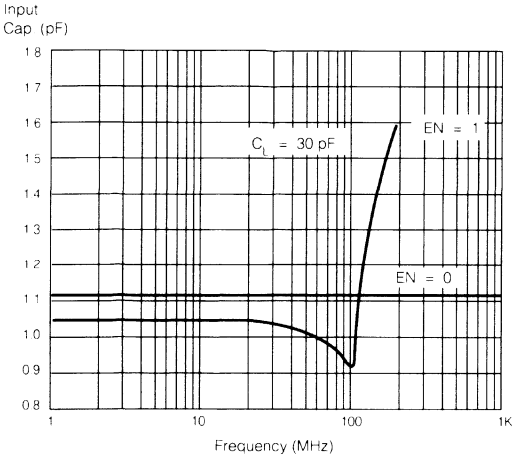


Fig. 5 C_{IN} vs Frequency

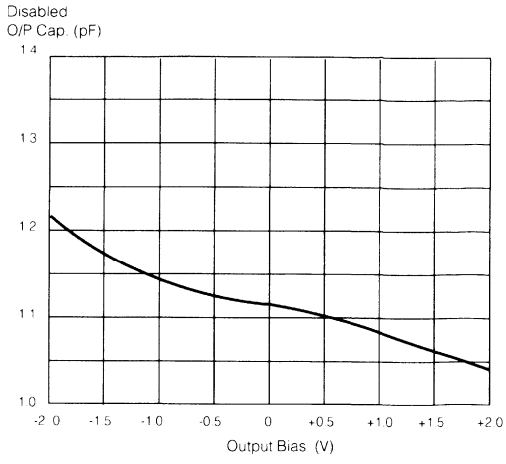


Fig. 6 C_{OUT} vs Bias

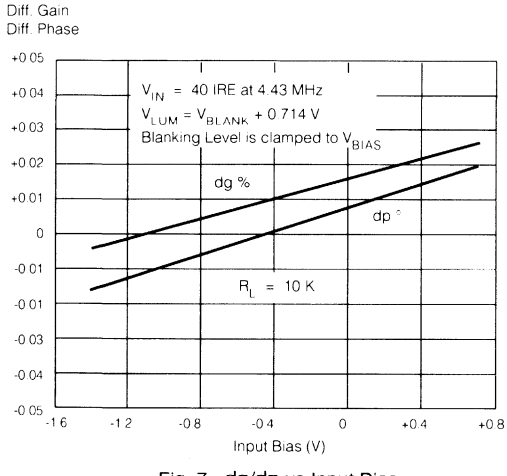


Fig. 7 dg/dp vs Input Bias

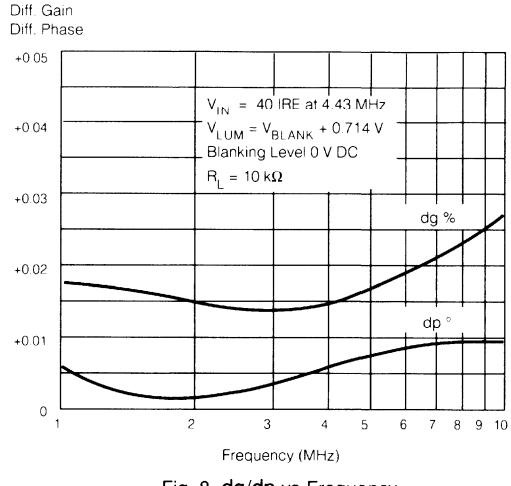


Fig. 8 dg/dp vs Frequency

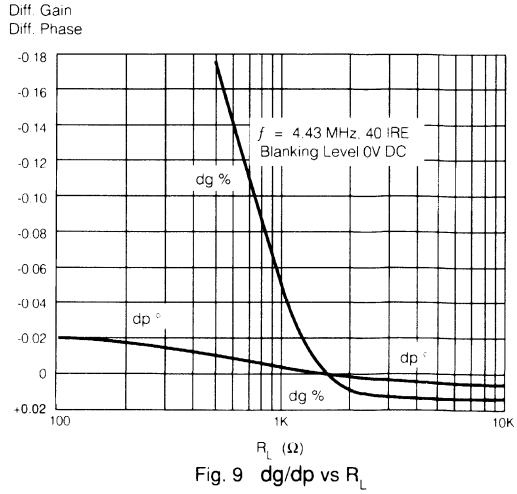


Fig. 9 dg/dp vs R_L

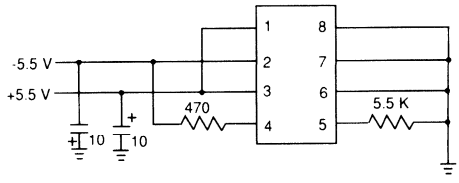


Fig. 10 Burn-in Test Circuit

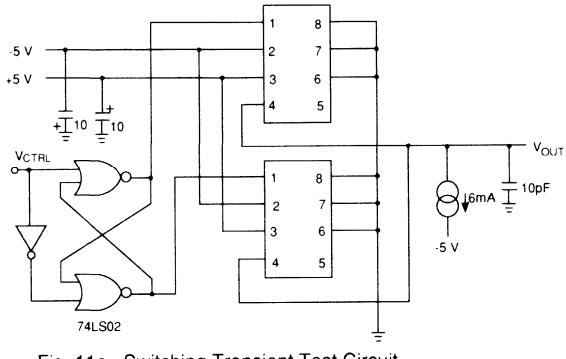


Fig. 11a Switching Transient Test Circuit

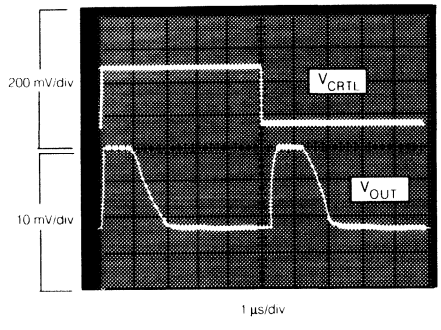
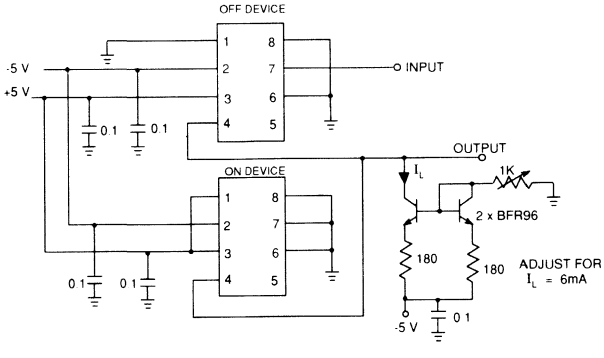
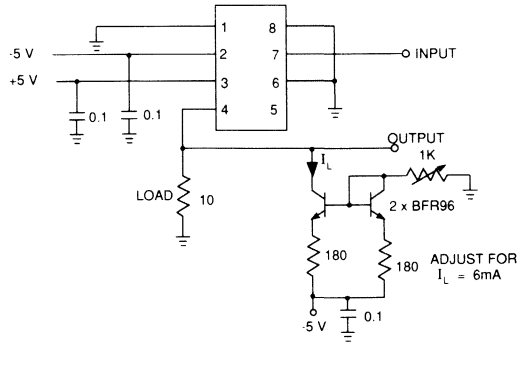


Fig. 11b Switching Transient



NOTE: Off-isolation can be increased by eliminating the signal path through the power supplies. This is demonstrated by replacing the enabled crosspoint with a 10Ω load resistor as shown in the passive load circuit.

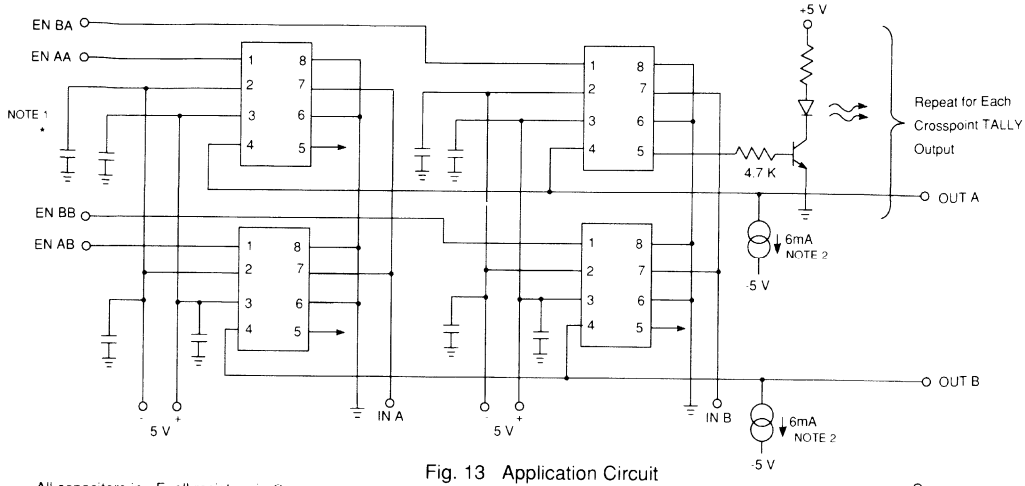
Active Load



Passive Load

Fig. 12 Off-isolation Test Circuits

All capacitors in µF, all resistors in Ω unless otherwise shown.

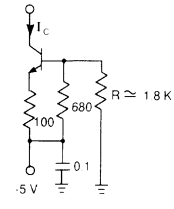


All capacitors in μF, all resistors in Ω unless otherwise shown.

Fig. 13 Application Circuit
2 x 2 Matrix using Four GX4201

NOTES: 1. * All decoupling capacitors are 0.1 μF, 50 V.

2. 6mA can be implemented by the following circuit. Choose a transistor with β / f_T at 6 mA f_T is ≥ 800MHz.



3. Alternatively, an 820Ω resistor may be used. The insertion loss will be increased to 0.1 dB.

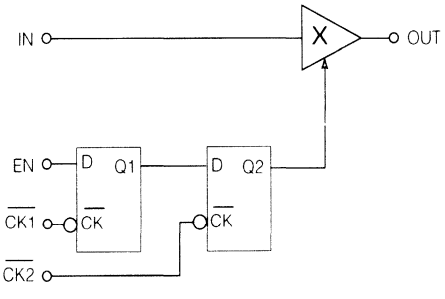
Wideband, Monolithic 1x1 Video Crosspoint Switch

GX4301 TENTATIVE DATA SHEET

FEATURES

- -3 dB bandwidth, 300 MHz with C_L = 0 pF
- off isolation at 100 MHz, 80 dB
- differential phase and gain at subcarrier 0.01° & 0.01%
- 1.65 mW disabled power consumption (± 5V Supplies)
- input signal levels from -2 V to +3 V (± 5V Supplies)
- dual, transparent control latches
- ± 5V to ± 12V supply voltage range

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

EN	$\overline{CK1}$	$\overline{CK2}$
0	0	1
0	0	0
1	0	1
1	0	0
X	1	1
X	1	0

Q1	Q2
0	$Q2_{n-1}$
0	0
1	$Q2_{n-1}$
1	1
$Q1_{n-1}$	$Q2_{n-1}$
$Q1_{n-1}$	$Q1_{n-1}$

Q2	OUT
0	HIGH Z
1	IN

X = DON'T CARE

CIRCUIT DESCRIPTION

The GX4301 is a wideband 1x1 video crosspoint implemented in bipolar monolithic technology. The device is characterized by excellent differential gain and phase in the enabled state, and very high off-isolation in the disabled state. The fully buffered unilateral signal path ensures negligible output to input feedback while delivering minimal output switching transients through make-before-break switching.

For use in NxM routing matrices, the device features a very high, nearly constant input impedance, coupled with very high output impedance in the disabled state. This allows multiple GX4301's to be paralleled at the input and output without additional circuitry.

To maximize system bandwidth, an external current source is used to bias the output device of the crosspoint. One external current source is required per output bus. For less demanding applications, a load resistor can be used in place of the output current source, causing a slight increase in differential phase. Non-additive mixing will occur on the output bus if more than one paralleled GX4301 is enabled at a time.

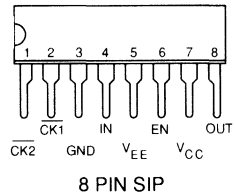
Dual transparent latches allow asynchronous addressing and synchronous switching. The control microprocessor can write to the input latch using $\overline{CK1}$, while the video timing clock can be used to initiate switching using $\overline{CK2}$. Alternatively, one or both of the latches can be made transparent by pulling CK1 or $\overline{CK2}$ low.

The GX4301 is one of a series of wideband video crosspoints utilizing Gennum's proprietary LSI process.

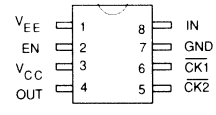
APPLICATIONS

- very high quality video switching
- HDTV switching and routing
- computer graphics
- RF switching/routing
- PCM/data routing

PIN CONNECTIONS



8 PIN SIP



8 PIN SOIC

Document No. 510 - 94

GENNUM CORPORATION P.O. Box 489, Stn A, Burlington, Ontario, Canada L7R 3Y3 tel. (416) 632-2996 fax: (416) 632-2055 telex: 061-8525
Japan Branch: 301 Aoba Building, 3-6-2 Takanawa, Minato-Ku, Tokyo 108, Japan tel. (03) 441-2096 fax: (03) 448-8991

ELECTRICAL CHARACTERISTICS (V_S = ±8V DC 0°C < T_A < 70°C, R_L = 10 kΩ, C_L = 30pF, I_L = 6mA)

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC SUPPLY	Supply Voltage	$\pm V_S$		4.5	-	13.2	V
	Supply Current (I_L of 6mA not included)	I+	Q2=1	-	11	-	mA
			Q2=0	-	200	-	µA
		I-	Q2=1	-	10	-	mA
			Q2=0	-	130	-	µA
STATIC	Analog Output Voltage Swing	V_{OUT}	Extremes before clipping occurs	-2	-	3	V
	Analog Input Bias Current	I_{BIAS}		-	12	-	µA
	Output Offset Voltage	V_{OS}	T_A = 25°C	-10	-	10	mV
LOGIC	Output Offset Voltage Drift-	$\Delta V_{OS} / \Delta T$		-	-	100	µV/°C
	Crosspoint selection Turn-On Time	t_{ON}	From $\overline{CK2}$	-	0.6	-	µs
			From EN.	-	0.8	-	µs
	Crosspoint selection Turn-Off Time	t_{OFF}	From $\overline{CK2}$	-	2.0	-	µs
			From EN	-	1.5	-	µs
	Clock Pulse Width	t_{OFF}		500	-	-	ns
	Logic Input Thresholds	V_{IH}	1	2.0	-	-	V
		V_{IL}	0	-	-	0.8	V
	Enable Input Bias Current	$I_{BIAS(EN)}$	EN = 1	-	0.1	-	µA
	$\overline{CK1}$/$\overline{CK2}$ Bias Current	$I_{BIAS(\overline{CK})}$	$\overline{CK}$ = 1	-	0.1	-	µA
DYNAMIC	Insertion Loss	I.L.	1V p-p sine or sq. wave at 100 kHz	-	0.025	-	dB
	Bandwidth (-3dB)	B.W.		-	300	-	MHz
	Gain Spread at 30 MHz			-	-	±0.1	dB
	Input Resistance	R_{IN}	Chip Selected	1	-	-	MΩ
	Input Capacitance	C_{IN}		-	1.1	-	pF
	Output Resistance	R_{OUT}		-	7	-	Ω
	Output Capacitance	C_{OUT}		-	1.1	-	pF
	Differential Gain	dg	at 3.58 MHz or 4.43 MHz	-	0.01	-	%
	Differential Phase	dp	V_{IN} = 40 IRE	-	0.01	-	degrees
	Off Isolation		Crosspoint on output to gnd, f = 100 MHz	-	80	-	dB
	Slew Rate	+SR	V_{IN} = 3V p-p (C_L = 0 pF)	250	400	-	V/µs
		-SR		250	350	-	

ABSOLUTE MAXIMUM RATINGS

Parameter	Value
Supply Voltage	±13.2 V
Operating Temperature Range	$0° C \leq T_A \leq 70° C$
Storage Temperature Range	$-65° C \leq T_S \leq 150° C$
Lead Temperature (Soldering, 10 Sec)	260° C
Analog Input Voltage	V_{EE} or $(V_{CC} - 14.2V) \leq V_{IN} \leq V_{CC}$ or $(V_{EE} + 16V)$
Logic Input Voltage	$-0.5 V \leq V_L \leq 5.5 V$
Output Load Current	12mA

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

AVAILABLE PACKAGING

8 pin SIP
8 pin Molded SOIC

Fast Toggling Video Crosspoint Switch

GY4102 TENTATIVE DATA SHEET

FEATURES

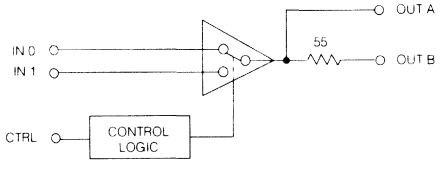
* 25 ns switching time (toggle)
* make-before-break switching
* 300 MHz at -3dB, bandwidth
* typically 0.03 dB insertion loss at 1 MHz
* typically 0.01 % differential gain at 3.58 MHz
* typically 0.01 degree differential phase at 3.58 MHz

CIRCUIT DESCRIPTION

The GY4102 is a bipolar, monolithic SPDT video switch incorporating fast control logic. The analog signal path is characterised by low differential gain, low differential phase and low insertion loss, coupled with a -3 dB bandwidth of typically 300 MHz into a 10 pF load.

Fast set-up times in the order of 20 nanoseconds allow toggling of video or data up to 20 MHz. The control input is TTL and 5 V CMOS compatible. The GY4102 is available in an 8 pin DIP.

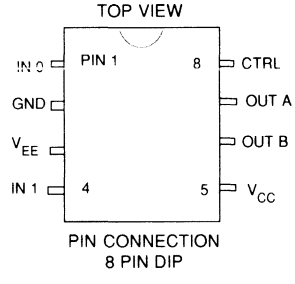
FUNCTIONAL BLOCK DIAGRAM



Patents Pending

APPLICATIONS

* Sub-pixel video switching
* Fast data sampling
* Modulation
* Special Effects video switching



PIN CONNECTION
8 PIN DIP

ABSOLUTE MAXIMUM RATINGS

Parameter	Value
Positive Supply Voltage	±6.0 V
Operating Temperature Range	0°C to 70° C
Storage Temperature Range	-65°C to 150° C
Lead Temperature (Soldering, 10 Sec)	260° C
Analog Input Voltage (IN 0, IN 1)	$V_{EE} < V_{IN} < V_{CC}$ +0.3 V
Control Input Voltage Range	-5 V < V_{CTRL} < V_{CC}+0.3 V

TRUTH TABLE

CTRL	OUTPUT*
0	IN 0
1	IN 1

* A or B

GENNUM CORPORATION P.O. Box 489, Stn A, Burlington, Ontario, Canada L7R 3Y3 tel. (416) 632-2996 fax: (416) 632-2055 telex: 061-8525
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ELECTRICAL CHARACTERISTICS

(V_S = ±5V DC, T_A = 0 - 70°C, C_L = 0pF Unless otherwise shown)

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC SUPPLY	Supply Voltage	V_S		4.5	5	5.5	V
	Supply Current	I+		-	20	-	mA
		I-		-	21	-	mA
LOGIC	Control Input Bias	I_{CTRL}	Control = 1	-	5	-	µA
	Logic Level threshold	V_{LOGIC}	1	2	-	-	V
			0	-	-	0.8	V
STATIC	Analog Input Bias Current	I_{BIAS}	Selected channel	-	11	-	µA
			Deselected channel	-	25	-	µA
	Output Voltage Swing	V_O		-1.2	-	+3	V
	Output Offset Voltage	V_{OS}	T_A = 25°C	-10	-	+10	mV
	Output Offset Drift	$\Delta V_{OS}/T$		-	5	-	µV/°C
DYNAMIC	Insertion Loss	I.L.	f = 100 kHz	-	0.03	-	dB
	Differential Gain	dg	f = colorburst 3.58 or 4.43 MHz	-	0.01	-	%
	Differential Phase	dp	f = colorburst 3.58 or 4.43 MHz	-	0.01	-	degrees
	Crosstalk	XTALK	f = 10 MHz	-	85	-	dB
	Bandwidth	f_{3dB}	C_L = 10 pF R_S = 55 Ω	100	300	-	MHz
	Slew Rate	+SR	V_{IN}= 2 Vp-p T_A = 25°C	-	430	-	V/µs
		-SR		-	320	-	V/µs

SWITCHING CHARACTERISTICS

(V_S = ±5V, T_A = 0 - 70°C, C_L =10pF, R_S = 55Ω)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Delay Time (see figure 1)	$t_{d\ (on)}$	Control input to output high (90%) 0 to 1 V transition	-	11	-	ns
	$t_{d\ (off)}$	Control input to output low (10%) 1 to 0 V transition	-	21	-	ns
Settling Time (see figure 2a)	$t_{S\ (on)}$	To 0.5 IRE on 0 to 1 V output, T_A = 25°C	-	7	-	ns
(see figure 2b)	$t_{S\ (off)}$	To 0.5 IRE on 1 to 0 V output, T_A = 25°C	-	3	-	ns
Switching Transient		Amplitude (unfiltered) C_L = 0pF	-	35	50	mV
		Duration (unfiltered) C_L = 0pF	-	2.3	4	ns

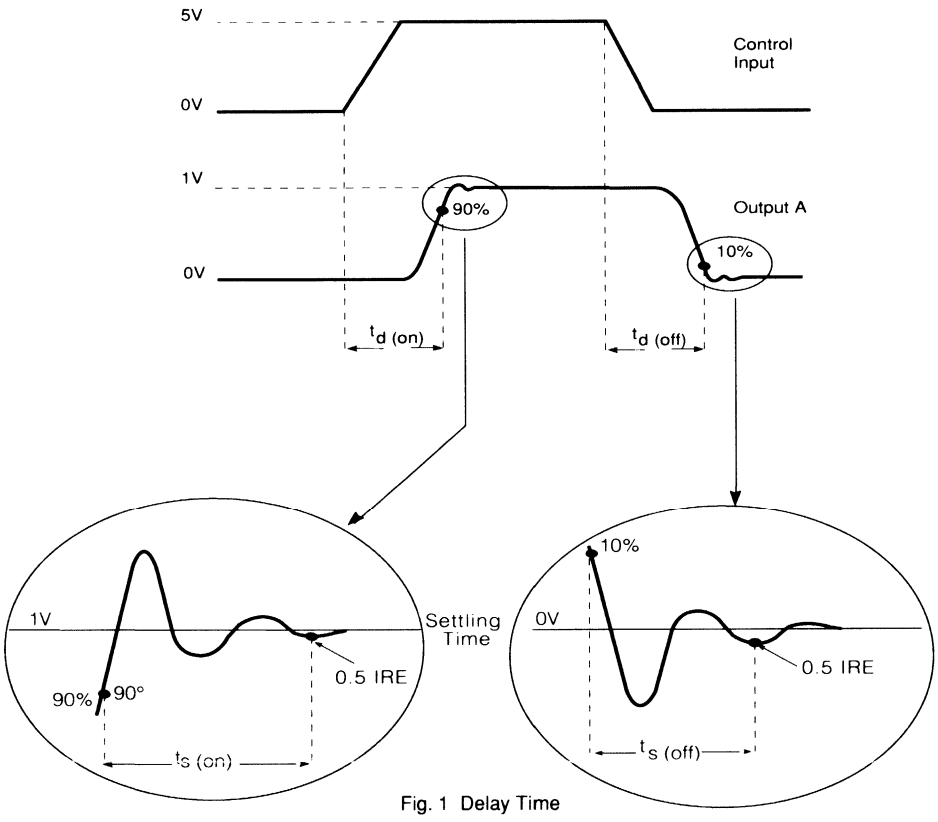


Fig. 1 Delay Time

AVAILABLE PACKAGING

8 pin DIP

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

Revision date March1990

Monolithic 4x1 Video Crosspoint Switches

GX414, GX424, GX434 DATA SHEET

FEATURES

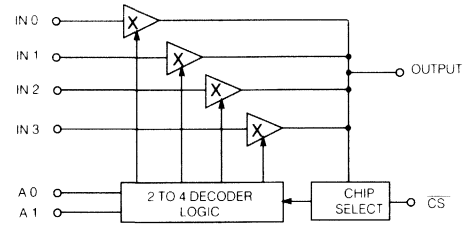
- **low differential gain: 0.03% typ. at 4.43 MHz**
- **low differential phase: 0.012 deg. typ. at 4.43 MHz**
- **low insertion loss: 0.05 dB max at 100 kHz**
- **low disabled power consumption: 5.2 mW typ.**
- **high off isolation: 110 dB at 10 MHz**
- **all hostile crosstalk @ 5 MHz, 97 dB typ.**
- **bandwidth (-3dB) with 30 pF load, 100 MHz typ.**
- **fast make-before-break switching: 200 ns typ.**
- **TTL and 5 volt CMOS compatible logic inputs**
- **low cost 14 pin DIP and16 pin SOIC packages**
- **optimised performance for NTSC, PAL and SECAM applications**

APPLICATIONS

Glitch free analog switching for...

- * High quality video routing
- * A/D input multiplexing
- * Sample and hold circuits
- * TV/ CATV/ monitor switching

FUNCTIONAL BLOCK DIAGRAM



Patents Pending

TRUTH TABLE

$\overline{CS}$	A1	A0	OUTPUT
0	0	0	IN 0
0	0	1	IN 1
0	1	0	IN 2
0	1	1	IN 3
1	X	X	HI - Z

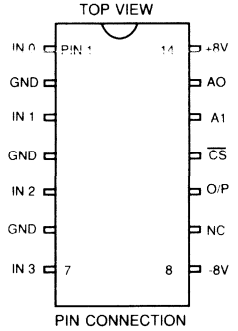
X = DON'T CARE

CIRCUIT DESCRIPTION

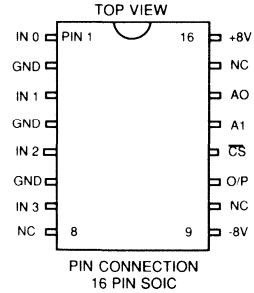
The GX414, GX424 and GX434 are high performance low cost monolithic 4x1 video crosspoints incorporating four bipolar switches with a common output, a 2 to 4 address decoder and fast chip select circuitry. The chip select input allows for multi-chip paralleled operation in routing matrix applications. The chip is selected by applying a logic 0 on the chip select input.

Unlike devices using MOS bilateral switching elements, these bipolar circuits represent fully buffered, unilateral transmission paths when selected. This results in extremely high output to input isolation. They also feature fast make-before-break switching action. These features eliminate such problems as switching 'glitches' and output-to-input signal feedthrough.

This family of devices operates from ±7 to ± 13.2 volt DC supplies. They are specifically designed for video signal switching which requires extremely low differential phase and gain. Logic inputs are TTL and 5 volt CMOS compatible providing address and chip select functions. When the chip is not selected, the output goes to a high impedance state.

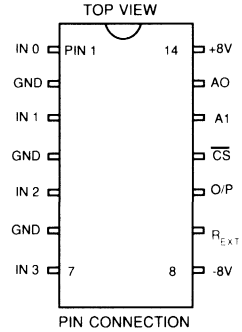


PIN CONNECTION
14 PIN DIP

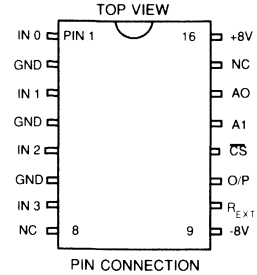


PIN CONNECTION
16 PIN SOIC

GX414,GX424



PIN CONNECTION
14 PIN DIP



PIN CONNECTION
16 PIN SOIC

GX434

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ABSOLUTE MAXIMUM RATINGS

Parameter	Value & Units
Supply Voltage	±13.5V *
Operating Temperature Range	0°C ≤ T_A ≤ 70° C
Storage Temperature Range	-65°C ≤ T_S ≤ 150° C
Lead Temperature (Soldering, 10 Sec)	260° C
Analog Input Voltage	-4V ≤ V_{IN} ≤ +2.4V
Analog Input Current	50µA AVG, 10 mA peak
Logic Input Voltage	-4V ≤ V_L ≤ +5.5V **

* ±10V**, +5V, GX424 only

ORDERING INFORMATION

Part Number	Package Type	Temperature Range
GX414 - - CDB	14 Pin DIP	0° to 70° C
GX414 - - CKC	16 Pin SOIC	0° to 70° C
GX424 - - CDB	14 Pin DIP	0° to 70° C
GX424 - - CKC	16 Pin SOIC	0° to 70° C
GX434 - - CDB	14 Pin DIP	0° to 70° C
GX434 - - CKB	16 Pin SOIC	0° to 70° C

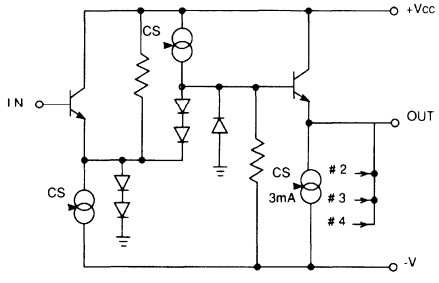


Fig.1 Crosspoint Equivalent Circuit

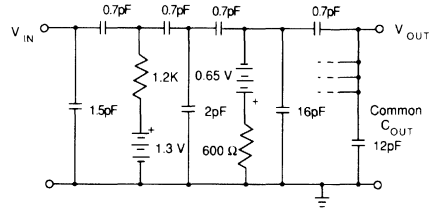


Fig. 2 Disabled Crosspoint Equivalent Circuit

ELECTRICAL CHARACTERISTICS (V_S = ±8V DC, 0°C < T_A < 70°C, C_L = 30 pF, R_L = 10kΩ unless otherwise shown)

				GX414			GX424			GX434†			
	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DC SUPPLY	Supply Voltage	±V_S		7	8	13.2	7	8	10	7	8	13.2	V
	Supply current	I+	Chip selected ($\overline{CS}$=0)	-	11	14	-	11	18	-	10.5	11.5	mA
			Chip not selected ($\overline{CS}$=1)	-	0.4	0.58	-	0.46	0.9	-	0.4	0.58	mA
		I-	Chip selected ($\overline{CS}$=0)	-	10.5	14	-	10.5	18	-	10.2	11.2	mA
			Chip not selected ($\overline{CS}$=1)	-	0.25	0.38	-	0.25	0.4	-	0.25	0.38	mA
STATIC	Analog Output Voltage Swing	V_{OUT}	Extremes before clipping occurs	- -	+2 -1.2	-	- -	+2 -1.2	-	- -	+2 -1.2	-	V
	Analog Input Bias Current	I_{BIAS}		-	22		-	22	-	-	22	-	µA
	Output Offset Voltage	V_{OS}	T_A = 25°C, 75 Ω resistor on each input to gnd	-2	5	12	-20	2	30	0	7	14	mV
	Output Offset Voltage Drift	$\Delta V_{OS}/\Delta T$		-	+50	+200	-	+50	+300	-	+50	+200	µV/°C

†R_{EXT} = 33.2 kΩ 1%

ELECTRICAL CHARACTERISTICS continued

(V_S = ±8V DC, 0°C < T_A < 70°C, C_L = 30pF, R_L = 10kΩ unless otherwise shown)

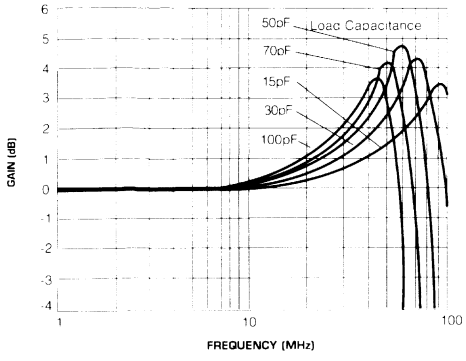
				GX414			GX424			GX434*			
	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
	Crosspoint Selection Turn-On Time	$t_{ADR\ ON}$	Control input to appearance of signal at the output	130	200	270	100	200	350	130	200	270	ns
	Crosspoint Selection Turn-Off Time	$t_{ADR\ OFF}$	Control input to disappearance of signal at output	390	600	800	300	600	950	390	600	800	ns
	Chip Selection Turn-On Time	$t_{CS\ ON}$	Control input to appearance of signal at output	200	300	400	150	300	450	200	300	400	ns
	Chip Selection Turn-Off Time	$t_{CS\ OFF}$	Control input to disappearance of signal at output	460	700	940	400	700	1100	460	700	940	ns
LOGIC	Logic Input Thresholds	V_{IH}	1	2.0	-	-	2.0	-	-	2.0	-		V
		V_{IL}	0	-	-	1.1	-	-	1.1	-	-	1.1	V
	Address Input Bias Current	$I_{BIAS(ADR)}$	Chip selected: A0,A1 = 1	-	-	5.0	-	-	5.0	-	-	5.0	µA
			Chip selected: A0,A1 = 0	-	-	0.1	-	-	0.1	-	-	0.1	nA
	Chip Select Bias Current	$I_{BIAS(\overline{CS})}$	$\overline{CS}$ = 1	-	-	1.0	-	-	1.0	-	-	1.0	nA
			$\overline{CS}$ = 0	-	-	30	-	-	30	-	-	30	µA
DYNAMIC	Insertion Loss	IL	1V p-p sine or sq. wave at 100 kHz	0.02	0.03	0.05	0.015	0.03	0.06	0.025	0.03	0.04	dB
	Bandwidth (-3 dB)	BW		90	100	-	80	100	-	100	120	-	MHz
	Gain Spread at 8 MHz			-	-	±0.1	-	-	+0.46 -0.12	-	-	+0.06 -0.04	dB
	Input to Output Signal Delay Matching (chip to chip)	Δt_p	T_A = 25°C, R_S = 75Ω, f = 3.579545 MHz	-	-	±0.35	-	-	±0.8	-	-	±0.15	degrees
			0°C < T_A < 70°C, R_S as above, f as above	-	-	±0.7	-	-	±1.2	-	-	±0.3	degrees
	Input Resistance	R_{IN}	Chip selected ($\overline{CS}$ = 0)	900	-	-	900	-	-	900	-	-	kΩ
	Input Capacitance	C_{IN}	Chip selected ($\overline{CS}$ = 0)	-	2.0	-	-	2.0	-	-	2.0	-	pF
			Chip not selected ($\overline{CS}$ = 1)	-	2.4	-	-	2.4	-	-	2.4	-	pF
	Output Resistance	R_{OUT}	Chip selected ($\overline{CS}$ = 0)	-	14	-	-	14	-	-	14	-	Ω
	Output Capacitance	C_{OUT}	Chip not selected ($\overline{CS}$ = 1)	-	15	-	-	15	-	-	15	-	pF
	Differential Gain	dg	at 3.579545 MHz, V_{IN} = 40 IRE (Fig. 7)	-	0.03	0.05	-	0.03	0.1	-	0.03	0.05	%
	Differential Phase	dp		-	0.012	0.025	-	0.012	0.05	-	0.012	0.025	degrees
	All Hostile Crosstalk (see graph)	$X_{TALK(AH)}$	Sweep on 3 inputs 1V p-p, 4th input has 10 Ω resistor to gnd, f = 5 MHz (Fig. 6)	94	97	-	92	97	-	94	97	-	dB
	Chip Disabled Crosstalk (see graph)	$X_{TALK(CD)}$	f = 10 MHz (Fig. 5)	100	110	-	90	110	-	100	110	-	dB
	Slew Rate	+SR	V_{IN} = 3V p-p (C_L = 0 pF)	84	120	-	60	120	-	360	450	-	V/µs
		-SR		70	100	-	50	100	-	160	200	-	V/µs

* R_{EXT} = 33.2kΩ, 1%

CAUTION

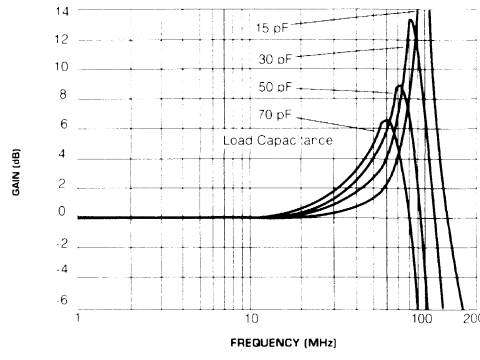
ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE DEVICES EXCEPT AT A STATIC-FREE WORKSTATION

GX414 GX424



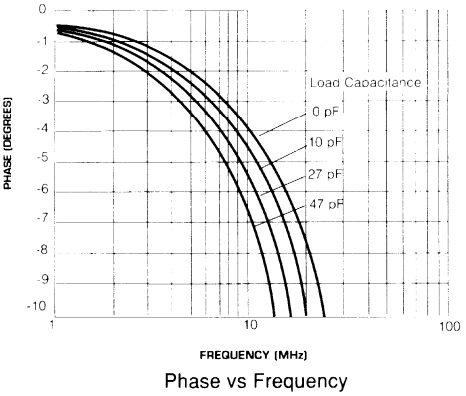
Gain vs Frequency

GX434



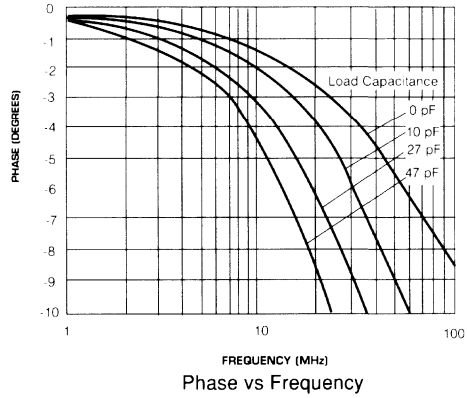
Gain vs Frequency

GX414 GX424



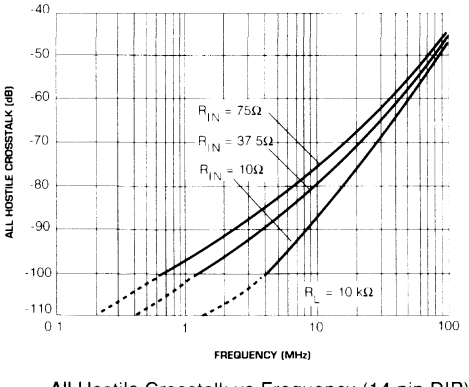
Phase vs Frequency

GX434

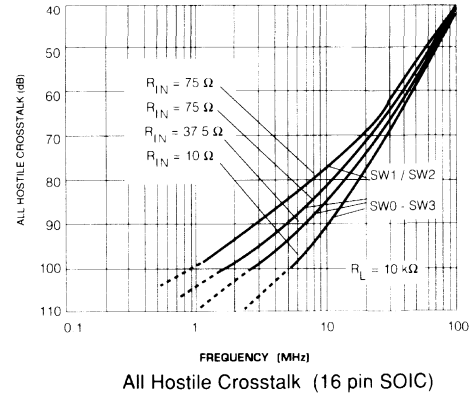


Phase vs Frequency

GX414 GX424 GX434



All Hostile Crosstalk vs Frequency (14 pin DIP)

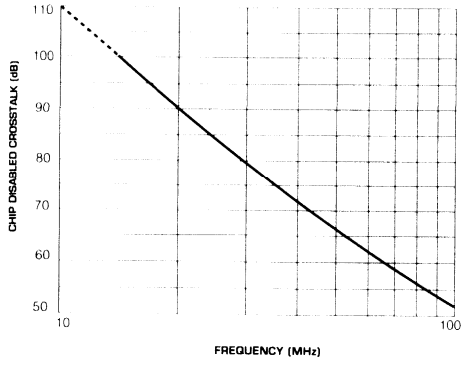


All Hostile Crosstalk (16 pin SOIC)

TYPICAL PERFORMANCE CURVES OF THE GX414, GX424 AND GX434

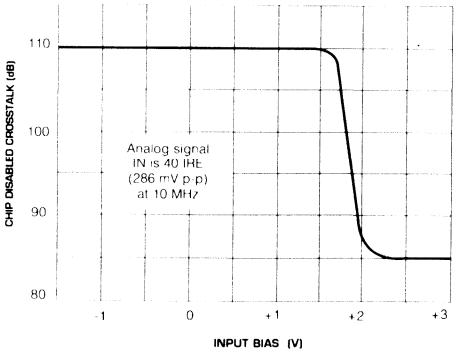
For all graphs, V_S = ±8 V DC and T_A = 25°C. The curves shown above represent typical batch sampled results.

GX414 GX424 GX434



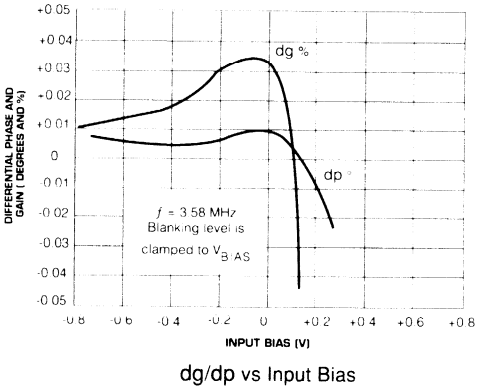
Chip Disabled Crosstalk vs Frequency

GX414 GX424 GX434



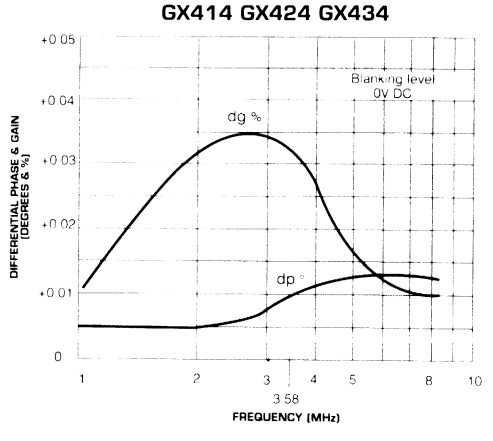
Chip Disabled Crosstalk vs Input Bias

GX414 GX424 GX434



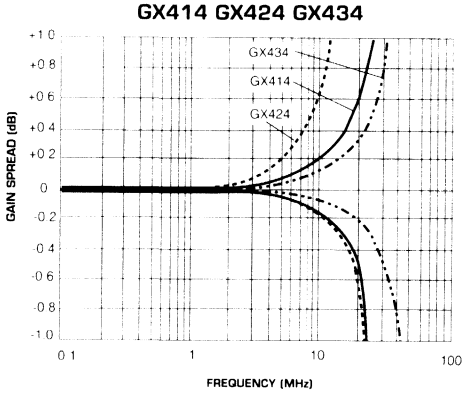
dg/dp vs Input Bias

GX414 GX424 GX434



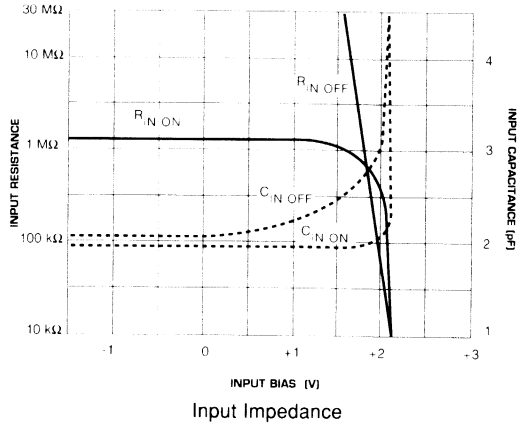
dg/dp vs Frequency

GX414 GX424 GX434



Normalized Gain Spread C_L = 30pF

GX414 GX424 GX434



Input Impedance

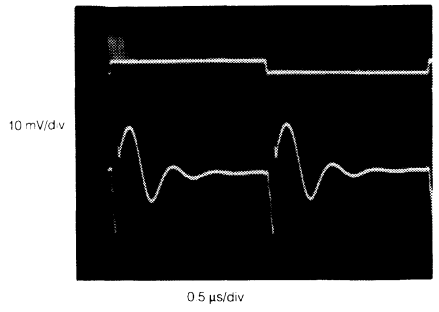


Fig.3 Switching Transient (crosspoint to crosspoint)

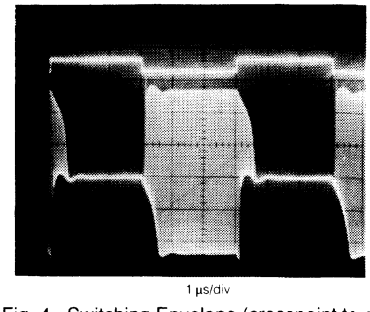


Fig. 4 Switching Envelope (crosspoint to crosspoint)

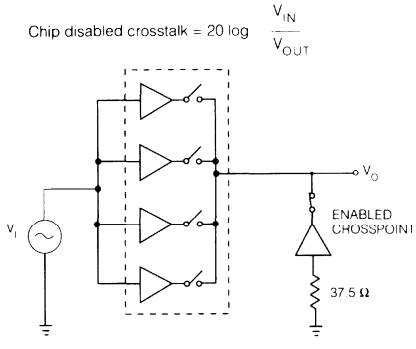


Fig. 5 Chip Disabled Crosstalk Test Circuit

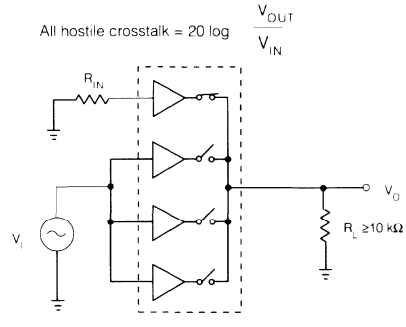


Fig. 6 All Hostile Crosstalk Test Circuit

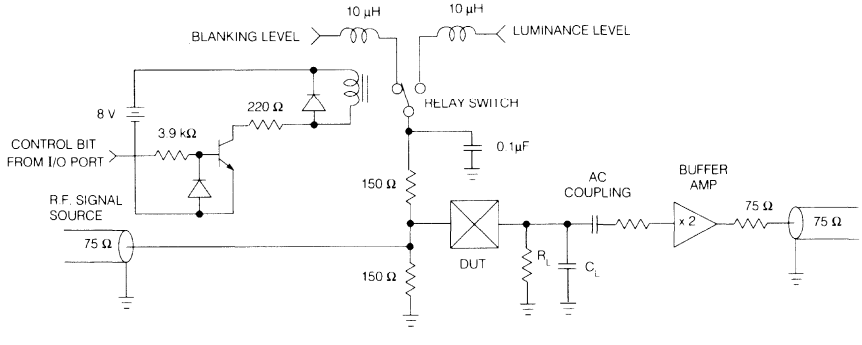


Fig. 7 Differential Phase and Gain Test Circuit

DIFFERENTIAL GAIN AND PHASE TEST CIRCUIT

The test circuit of Figure 7 allows two DC bias levels, set by the user, to be superimposed on a high frequency signal source. A computer controlled relay selects either the preset blanking or luminance level. One measurement is taken at each level and the change in gain or phase is calculated. This procedure is repeated one hundred times to provide a reasonably large sample.

The results are averaged to reduce the standard deviation and therefore improve the accuracy of the measurement.

The output from the device under test is AC coupled to a buffer amplifier which allows the buffer to operate at a constant luminance level so that it does not contribute any dg or dp to the measurement.

OPTIMISING THE PERFORMANCE OF THE GX414, GX424 AND GX434

1. Power Supply Considerations

Table 1 shows the effect on differential gain (dg) and differential phase (dp) of various power supply voltages that may be used. A nominal supply voltage of ±8 volts result in parameter values as shown in the top row of the table. By using other power supply voltage combinations, improvements to these parameters are possible at the sacrifice of increased chip power dissipation. Maximum degradation of the differential gain and phase occurs for the last combination of +12 , -7 volts along with an increase in power dissipation; these voltages are not recommended.

Supply Voltage	Differential Gain % (Typical)	Differential Phase degrees (Typical)
±8	0.030	0.012
+8/ -12	0.010	0.007
±12	0.010	0.007
+12/ -7	0.084	0.080

Table 2 shows the general characteristic variations of the GX4 family when different combinations of power supply voltages are used. These changes are relative to a circuit using ± 8 volts Vcc.

Supply Voltage	Characteristic Changes
± /	- lower logic thresholds - max logic I/P (≈ 4.5V) - loss of off isolation (≈20 dB) - poorer dg and dp
+8/ -12	- slight increase in negative supply current - slight decrease in offset - very similar frequency response - better dg and dp
±12	- increase in supply current (10%) - increase in offset (≈ 2-4 mV) - very similar frequency response - better dg and dp
+12/ -7	- loss in off isolation (≈20 dB) - poorer dg and dp

These devices do not require input DC biasing to optimise dg or dp nor do they need switching transient suppression at the output. Furthermore, both the analog signal and logic circuits within the chip use one common power supply, making power supply configurations relatively simple and straightforward. Several of the input characteristic graphs on pages 4-5 show that for best operation, the input bias should be 0 volts. The switching transient photographs on page 6 show how small the actual transients are and clearly show the make-before-break action of the GX4 family of video crosspoint switches.

2. Frequency Response Considerations

At frequencies higher than1 MHz, the output impedance of the crosspoint switches can be modelled as a voltage generator having a series resistance and a series inductance. The gain/ frequency characteristics exhibit peaking above 10 MHz due to the internal equivalent series inductance combined with any load capacitance. The peaking can be reduced by adding external series resistance to the output of the crosspoint. Figure 8 shows the effect of adding a 33Ω resistor to the output of a circuit having 47 pF effective load capacitance. This amount of load capacitance represents the equivalent of a 16 x1 crosspoint configuration using four ICs. Even though the frequency response has been flattened, the differential phase and gain have now changed as shown in Figure 9.

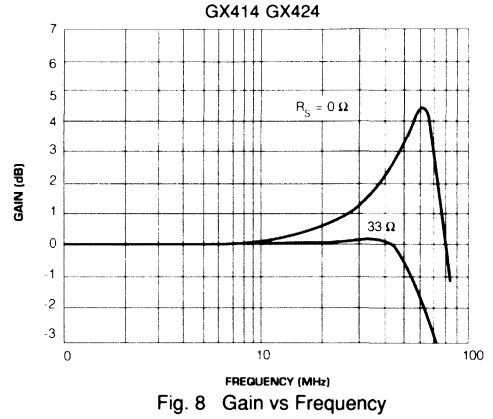


Fig. 8 Gain vs Frequency

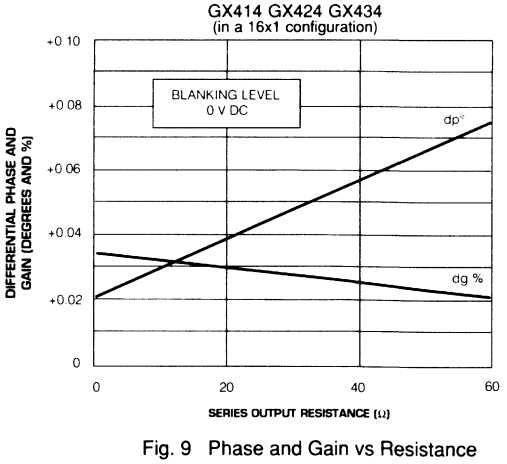


Fig. 9 Phase and Gain vs Resistance

The internal circuitry of the GX434 has been modified slightly in order to widen the bandwidth. This results in more peaking but the peaking frequency is higher. The response can be flattened by using an external series resistor. Test results yield a value of approximately 38Ω for a 16 x 1 configuration.

3. Load Resistance Considerations

This family of crosspoint switches are optimised for load resistances equal to or greater than 3 kΩ. Figure 10 shows the effect on the differential gain and phase when the load resistance is varied from 100 Ω to 100 kΩ.

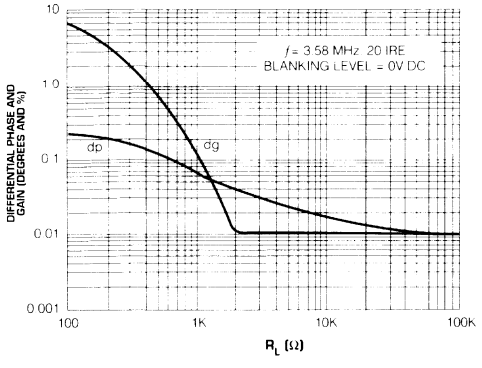


Fig. 10 dg/dp vs R_L

The negative slew rate is dependant upon the output current and load capacitance as shown below.

$$-SR = \frac{I + 3\ mA}{C_L} \qquad I \leq 8\ mA$$

The current I is determined from the following equation:

$$I = \frac{-V_{EE}}{R} \qquad R \geq 1\ k\Omega$$

It is possible to increase the negative slew rate (-S.R.) and thus the large signal bandwidth, by adding a resistance from the output to - V_{EE}. This resistor increases the output current above the 3 mA provided by the internal current generator and increases the negative slew rate. The additional slew rate improving resistance must not be less than 1kΩ in order to prevent excessive currents in the output of the device. An adverse effect of utilising this negative slew rate improving resistor, is the increase in differential phase from typically 0.009° to 0.014°. Under these same conditions, the differential gain drops from typically 0.033 % to 0.021 %.

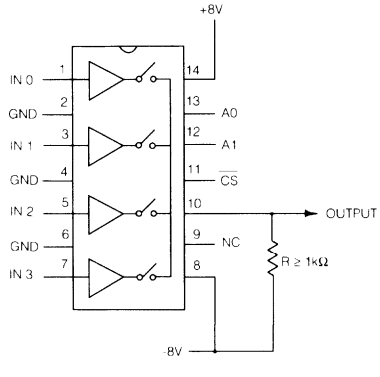


Fig.11 Negative Slew Rate (-SR) Improvement

4. Multi-chip Considerations

Whenever multi-chip bus systems are to be used, the total input and output capacitance must be carefully considered. The input capacitance of an enabled crosspoint (chip selected), is typically only 2 pF and increases slightly to 2.4 pF when the chip is disabled. The total output capacitance when the chip is disabled is approximately 15 pF per chip.

Usually the GX4 crosspoint switches are used in a matrix configuration of (n x 1) crosspoints perhaps combined in an (n x m) total routing matrix. This means for example, that four ICs produce a 16 x 1 configuration and have a total output capacitance of 4 x15 pF or 60 pF if all four chips are disabled. For any one enabled crosspoint, the effective load capacitance will be 3 x15 pF or 45 pF.

In a multi-input/multi-output matrix, it is important to consider the total input bus capacitance. The higher the bus capacitance and the more it varies from the ON to OFF condition, the more difficult it is to maintain a wide frequency response and constant drive from the input buffer. A 16 x 16 matrix using 64 ICs (16 x 4), would have a total input bus capacitance of 16 x 2.4 pF or 40 pF.

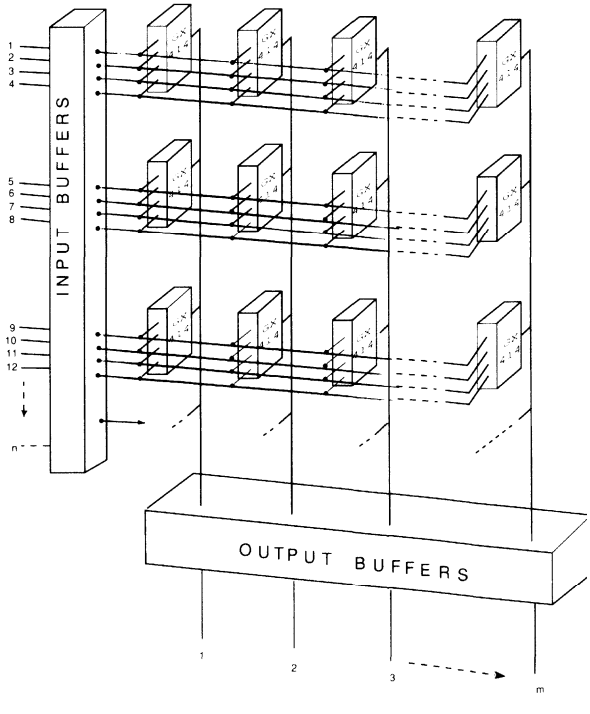


Fig.12 Multi-chip Connections

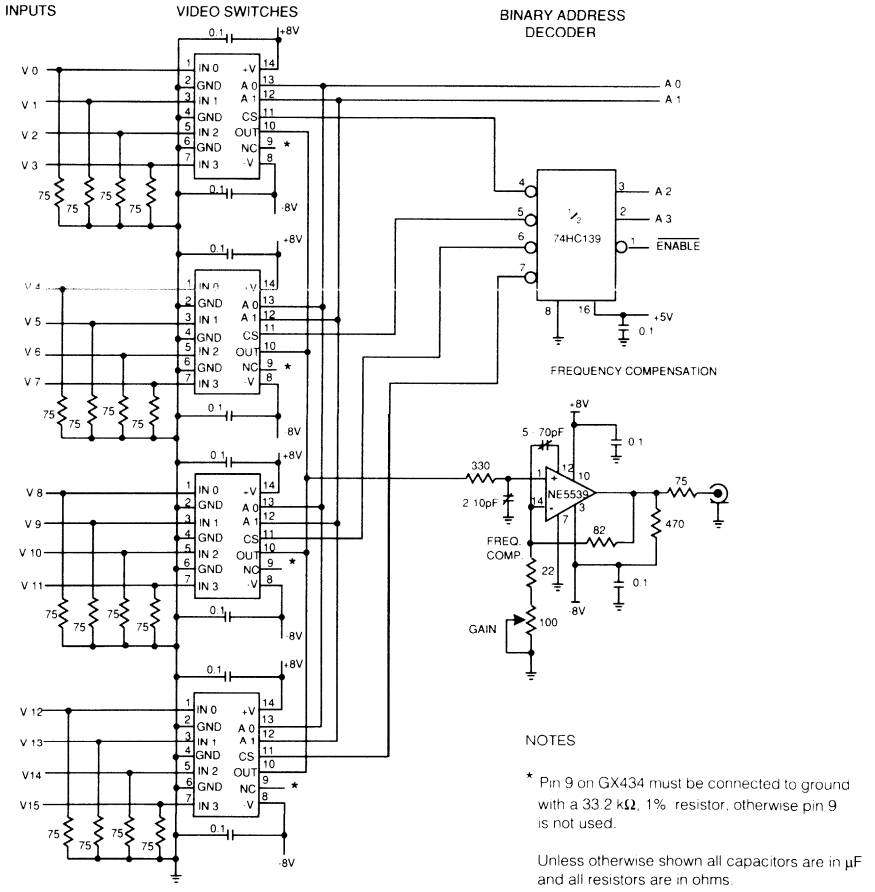
APPLICATIONS INFORMATION

The GX4 family of video switches are very high performance, wideband circuits requiring careful external circuit design. Good power supply regulation and decoupling are necessary to achieve optimum results. The circuit designer must use proper lead dress, component placement and PCB layout as in any high frequency circuit.

Functionally, the video switches are non-inverting, unity gain bipolar switches with buffered inputs requiring DC coupling and 75Ω line terminating resistors when directly driven from 75Ω cable. The output must be buffered to drive 75Ω lines. This is usually accomplished with the addition of an operational amplifier/ buffer which also allows adjustments to be made to the gain, offset and frequency response of the overall circuit. A typical video routing application is shown in Figure 13. Four ICs are used in a 16 x 1 crosspoint switching circuit.

An external address decoder is shown which generates the 16 address and chip enable codes from a binary number. The address inputs to each chip are active high while the chip select inputs are active low. Depending on the application and speed of the logic family used, latches may be required for synchronization where timing and delays are critical. Since the individual crosspoint switching circuits are unidirectional bipolar elements, low crosstalk and high isolation are inherent. The make-before-break switching characteristics of the GX414 means virtually 'glitch' free switching.

AVAILABLE PACKAGING
14 pin DIP and 16 pin SOIC



NOTES

* Pin 9 on GX434 must be connected to ground with a 33.2 kΩ, 1% resistor, otherwise pin 9 is not used.

Unless otherwise shown all capacitors are in μF and all resistors are in ohms.

Fig.13 16 x 1 Video Crosspoint Circuit

Monolithic 4x1 Video Crosspoint Switch

GX414A PRELIMINARY DATA SHEET

FEATURES

* low disabled power consumption: 5.2 mW
* low differential gain: 0.03% typ. at 4.43 MHz
* low differential phase: 0.012° typ. at 4.43 MHz
* bandwidth (-3dB) 100 MHz with 30 pF load
* all hostile crosstalk at 5 MHz -97dB typ.
* low insertion loss 0.05 dB max at 100 kHz
* off-isolation 110 dB at 10 MHz
* fast make before break switching: 200 ns typ.
* TTL and 5 volt CMOS compatible logic inputs
* for NTSC, PAL and SECAM applications
* low cost 14 pin DIP and16 pin SOIC packages

CIRCUIT DESCRIPTION

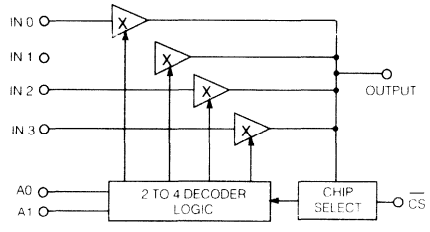
The GX414A is high performance low cost monolithic 4x1 video crosspoint switch incorporating four analog video switches and a 2 to 4 address decoder. An enabled input allows paralleled GX414As to be operated in a switching matrix with multiple inputs and a common output. Unlike similar devices using MOS bilateral switching elements, the GX414A represents a fully buffered unilateral transmission path when enabled. The GX414A requires ±8V and is designed for use in video switching applications. Logic inputs are TTL and 5V CMOS compatible, providing input select and output enable functions.

APPLICATIONS

Glitch free analog switching for...

* High quality video routing
* A/D input multiplexing
* Sample and hold circuits
* TV/ CATV/ monitor switching
* Instrumentation and communication equipment

FUNCTIONAL SCHEMATIC

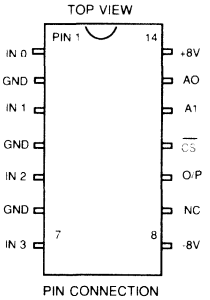


TRUTH TABLE

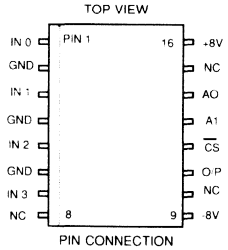
CS	A1	A0	OUTPUT
0	0	0	IN 0
0	0	1	IN 1
0	1	0	IN 2
0	1	1	IN 3
1	X	X	HI - Z

X = DON'T CARE

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION



PIN CONNECTION
14 PIN DIP



PIN CONNECTION
16 PIN SOIC

ORDERING INFORMATION

Part Number	Package Type	Temperature Range
GX414 - - ACDB	14 Pin DIP	0° to 70° C
GX414 - - ACKC	16 Pin SOIC	0° to 70° C

Document No. 510-19-1

GENNUM CORPORATION P.O. Box 489, Stn A, Burlington, Ontario, Canada L7R 3Y3 tel.(416) 632-2996 fax:(416) 632-2055 telex: 061-8525
JAPAN BRANCH: 301 Aoba Building, 3-6-2 Takanawa, Minato-ku, Tokyo 108, Japan tel. (03) 441-2096 fax: (03) 448-8991

ABSOLUTE MAXIMUM RATINGS

Parameter	Value
Supply Voltage	±13.5V
Operating Temperature Range	$0°C \le T_A \le 70°C$
Storage Temperature Range	$-65°C \le T_S \le 150°C$
Lead Temperature (Soldering, 10 Sec)	260° C

Parameter	Value
Analog Input Voltage	$-4V \le V_{IN} \le +2.4V$
Analog Input Current	50µA AVG, 10 mA peak
Logic Input Voltage	$-4V \le V_L \le +5.5V$

ELECTRICAL CHARACTERISTICS (V_S = ±8V DC, 0°C < T_A < 70°C, R_L = 10K, C_L = 30 pF, unless otherwise shown.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	$\overline{CS}$ = 0 V+	-	11	14	mA
	V-	-	10.5	14	
	$\overline{CS}$ = 1 V+	-	0.4	0.58	
	V-	-	0.25	0.38	
Analog Output Voltage Swing	Extremes before clipping occurs	-	+2.0	-	V
		-	-1.2	-	
Output Offset voltage	75Ω on each input ground	-2	5	12	mV
Output Offset Drift	$\Delta V_{OSC} / \Delta T$	-	+50	+200	µV / °C
Address Logic Delay	Control input to appearance of signal on output	130	200	270	ns
Chip Selection Delay	Control input to appearance of signal on output	200	300	400	ns
Logic Input Threshold	1	-	-	1.1	V
	0	2	-	-	V
Logic Input Current	A0, A1 = 1	-	-	5.0	µA
	A0, A1 = 0	-	-	0.1	nA
	$\overline{CS}$ = 1	-	-	1.0	nA
	$\overline{CS}$ = 0	-	-	30.0	µA
Insertion Loss	1V p-p sine or sq.wave at 100 kHz	0.02	0.03	0.05	dB
Gain Spread at 8 MHz		-	-	±0.25	dB
Bandwidth (-3dB)		90	100	-	MHz
Differential Gain	at 3.58 or 4.43 MHz	-	0.03	0.05	%
Differential Phase	at 3.58 or 4.43 MHz	-	0.012	0.025	degrees
Input to Output Delay Matching (chip-chip)	75Ω source impedance at 3.579545 MHz, T_A = 25°	-	-	±0.6	degrees
	75Ω source impedance at 3.579545 MHz, Full temp.	-	-	±1.0	degrees
All Hostile Crosstalk	Sweep on 3 inputs 1V p-p 4th input 10 Ω to gnd at 5 MHz	94	97	-	dB
Chip Disabled Crosstalk	14Ω on output to gnd at 10 MHz	100	110	-	dB
Input Resistance	$\overline{CS}$ = 0	-	960	-	kΩ
Input Capacitance	$\overline{CS}$ = 0	-	2.0	-	pF
	$\overline{CS}$ = 1	-	2.4	-	pF
Output Resistance	$\overline{CS}$ = 0	-	14	-	Ω
Output Capacitance	$\overline{CS}$ = 1	-	15	-	pF
Slew Rate	+SR	-	40	-	V/µs
	V_{IN} = 3V p-p (C_L = 0 pF) -SR	-	40	-	V/µs

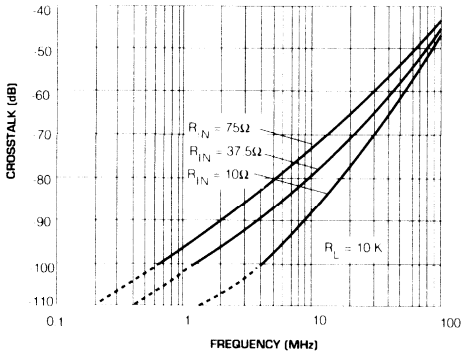


Fig. 1 Typical All Hostile Crosstalk Performance (14 pin DIP)

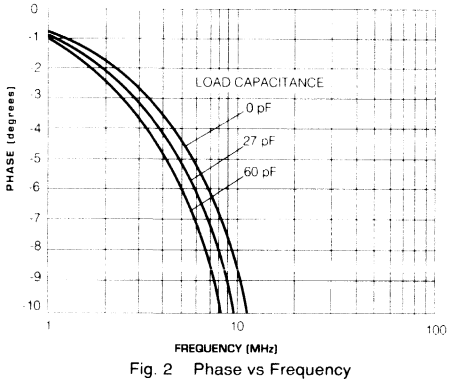


Fig. 2 Phase vs Frequency

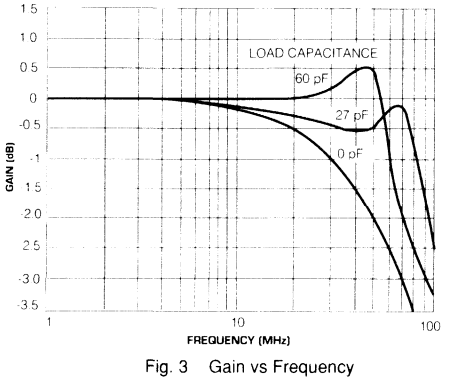


Fig. 3 Gain vs Frequency

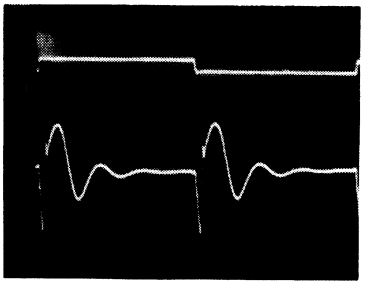


Fig. 4 Switching Transient (crosspoint-to-crosspoint)

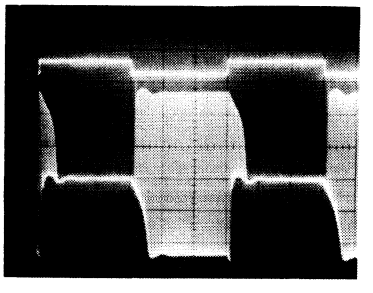


Fig. 5 Switching Envelope (crosspoint-to-crosspoint)

APPLICATION INFORMATION

As expected with any wide bandwidth circuit, the layout is critical. Good power supply regulation and bypassing are necessary, along with good high frequency design practice. Proper lead dress, component placement and PC board layout must be exercised for optimum performance.

The GX414A is non-inverting. Frequency peaking is compensated on-chip and optimised for a 60 pF load. The inputs are buffered and require 75Ω line terminating resistors when driven from 75Ω cable. The output must be buffered to drive 75Ω lines. The addition of an amplifier/buffer also allows adjustments to be made to the gain, offset and frequency response of the circuit. By reducing the load capacitance from 60 pF, the GX414A can be used to compensate for the frequency peaking of the buffer.

A typical application is shown in Figure 6 on the next page . Two GX414A devices are paralleled to form an 8x1 crosspoint switch. The three address lines make use of the A0, A1 and $\overline{CS}$ inputs. If more than two devices are used in parallel, a decoder will be necessary to generate the extra address inputs. Depending on the application and the speed of the logic family employed, latches may be required for synchronization where timing and delays are important.

The active switching circuitry of the GX414A will ensure low crosstalk and high performance over an input voltage range of -1.2 V to +2.0 V.

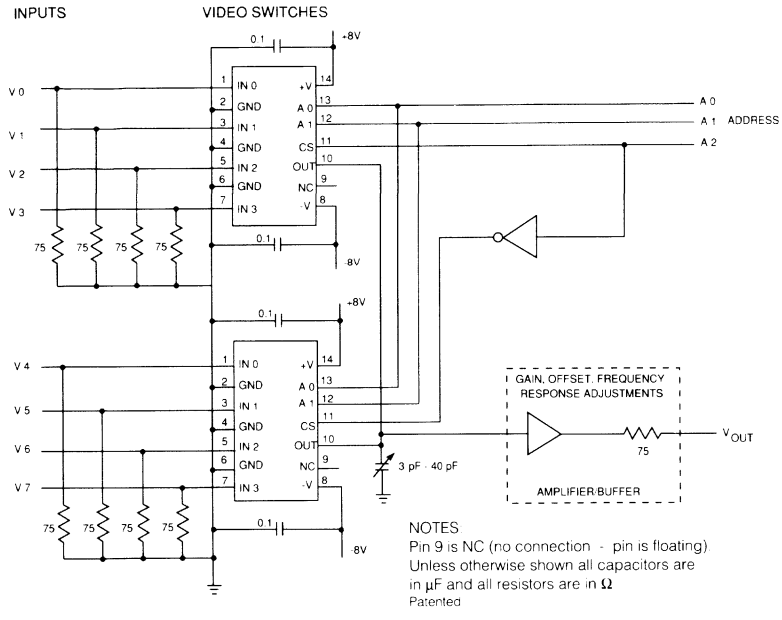


Fig. 6 Video Multiplexer Incorporating Two GX414A Circuits

AVAILABLE PACKAGING

14 pin DIP and 16 pin SOIC

GENNUM CORPORATION

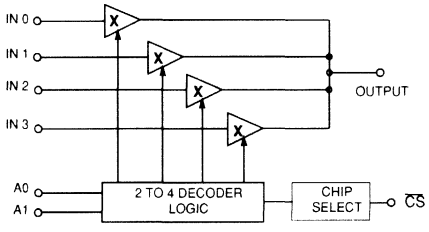
Monolithic 4x1Video Crosspoint Switch

GX214 PRELIMINARY DATA SHEET

FEATURES

* low cost
* differential gain at 3.58 MHz, 0.05% max.
* differential phase at 3.58 MHz, 0.05 deg. max.
* off-isolation better than 90 dB at 10 MHz
* all hostile crosstalk at 3.58 MHz, 75 dB typ. (R_{IN}= 75 Ω)
* make-before-break switching

FUNCTIONAL BLOCK DIAGRAM



Patents Pending

CIRCUIT DESCRIPTION

The GX214 is a low cost 4x1 video crosspoint switch containing four analog video switches and a 2 to 4 decoder. A Chip Select input allows paralleled GX214s to be operated in a switching matrix.

The GX214 represents a fully buffered, unilateral transmission path when enabled. When disabled, the output is high impedance.

The device operates from ±7.5 V to ±9.5 V supplies with TTL and 5 V CMOS compatible input logic levels.

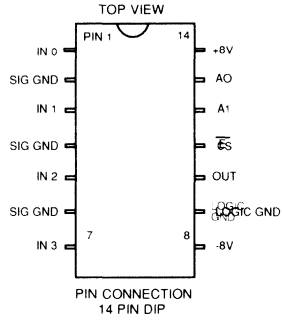
APPLICATIONS

* CATV and CCTV systems
* low cost video routing

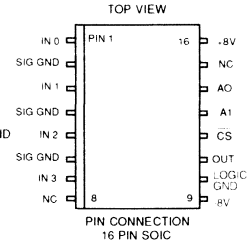
TRUTH TABLE

$\overline{CS}$	A1	A0	OUTPUT
0	0	0	IN 0
0	0	1	IN 1
0	1	0	IN 2
0	1	1	IN 3
1	X	X	HI - Z

X = DON'T CARE



PIN CONNECTION
14 PIN DIP



PIN CONNECTION
16 PIN SOIC

ORDERING INFORMATION

Part Number	Package Type	Temperature Range
GX214 - - CDB	14 Pin DIP	0° to 70°C
GX214 - - CKB	14 Pin SOIC	0° to 70°C
GX214 - - CKC	16 Pin SOIC	0° to 70°C

AVAILABLE PACKAGING

14 pin DIP, 14 pin SOIC and 16 pin SOIC

CAUTION

ELECTROSTATIC SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION

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JAPAN BRANCH: 301 Aoba Building, 3-6-2 Takanawa, Minato-ku, Tokyo 108, Japan tel. (03) 441-2096 fax: (03) 448-8991

ABSOLUTE MAXIMUM RATINGS

Parameter	Value
Supply Voltage	±10.0 V
Operating Temperature Range	0 °C ≤ T_A ≤ 70 °C
Storage Temperature Range	-65 °C ≤ T_S ≤ 150 °C

Parameter	Value
Lead Temperature (Soldering, 10 Sec)	260 °C
Analog Input Voltage	-4 V ≤ V_{IN} ≤ V_{CC}+0.3 V
Logic Input Voltage	0 V ≤ V_L ≤ 5.5 V

NOTE: A short from output to ground or either supply will destroy the device. For R_{EXT} use a 1.2 kΩ 1%, $^1/_4$ W resistor.

ELECTRICAL CHARACTERISTICS (V_S = ±8 V DC, 0°C < T_A < 70 °C, R_L = 1.21 kΩ to V_{EE}, C_L = 30pF)

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC SUPPLY	Supply Voltage	±V_S		7.5	8.0	9.5	V
	Supply Current	I+	Chip selected ($\overline{CS}$=0)	-	14	20	mA
			Chip not selected ($\overline{CS}$=1)	-	0.6	0.95	mA
		I-	Chip selected ($\overline{CS}$=0)	-	13	18	mA
			Chip not selected ($\overline{CS}$=1)	-	0.58	0.88	mA
STATIC	Analog Output Voltage Swing	V_{OUT}	Extremes before clipping occurs	-	-	+5.0 -1.2	V
	Analog Input Bias Current	I_{IN}		-	25	-	µA
	Output Offset Voltage	V_{OS}	75Ω resistor on each input to ground	-45	-80	-120	mV
LOGIC	Turn-On Time	t_{ON}	Control input to disappearance of signal at output.	700	900	1100	ns
	Turn-Off Time	t_{OFF}	Control input to disappearance of signal at output.	1.2	2.0	3.0	µs
	Logic Input Thresholds	V_{IH}	1	2.4	-	-	V
		V_{IL}	0	-	-	0.6	V
	Logic Input Bias Current	I_{BIAS}	Chip Selected A0,A1 = 1	-	-	10	nA
			Chip Selected A0,A1 = 0	-	-	60	µA
DYNAMIC	Insertion Loss	I.L.	1V p-p sine or sq. wave at 100 kHz	0.1	0.13	0.16	dB
	Bandwidth (-3dB)	B.W.		65	85	-	MHz
	Input Resistance	R_{IN}	Chip selected ($\overline{CS}$ = 0)	900	-	-	kΩ
	Input Capacitance	C_{IN}	Chip selected ($\overline{CS}$ = 0)	-	2.0	-	pF
			Chip not selected ($\overline{CS}$=1)	-	2.2	-	pF
	Output Resistance	R_{OUT}	Chip selected ($\overline{CS}$=0)	-	9	-	Ω
	Output Capacitance	C_{OUT}	Chip not selected ($\overline{CS}$=1)	-	12	-	pF
	Differential Gain	dg	at 3.58 MHz	-	-	0.05	%
	Differential Phase	dp	V_{IN} = 40 IRE	-	-	0.05	deg
	All Hostile Crosstalk	$X_{TALK(AH)}$	Sweep on 3 inputs 1V p-p 4th input has 75 Ω resistor to gnd. f = 10 MHz	73	75	-	dB
	Chip Disabled Crosstalk	$X_{TALK(CD)}$	One xpt on output to ground f = 10 MHz	90	100	-	dB

APPLICATION INFORMATION

The circuit layout of any wideband circuit is critical. Good high frequency design practice, proper lead dress and PCB component placement along with a well regulated and decoupled power supply will assure optimum performance of the crosspoint.

The GX214 is non-inverting. The inputs are buffered and require 75Ω line terminating resistors when driven from 75Ω cable. The inputs may be driven directly from an amplifier which has low output impedance.

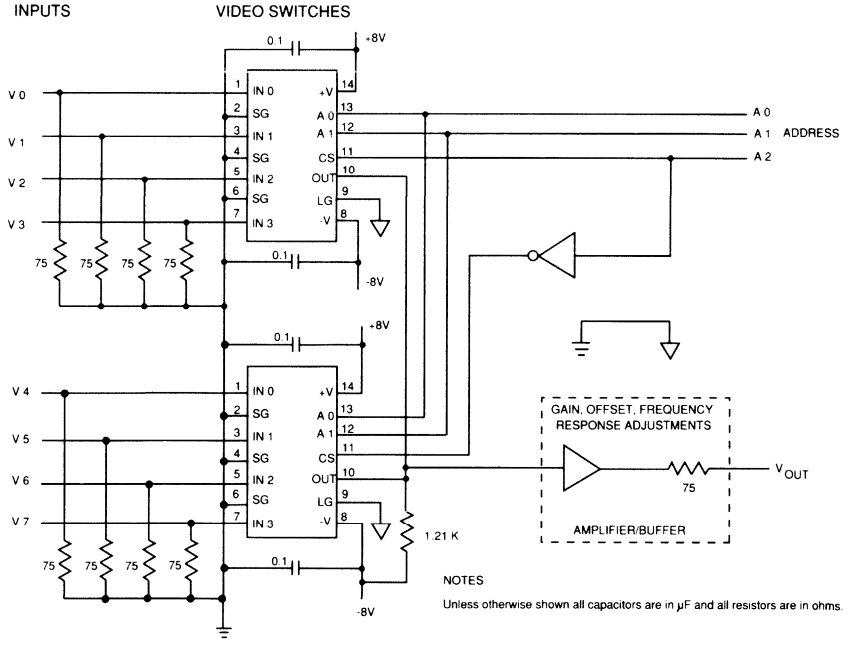
The output of the GX214 must be buffered to drive 75 Ω lines. The addition of an amplifier/buffer also allows adjustments to be made to the gain, offset and frequency response of the circuit.

Signal Ground (SG) pins 2, 4 and 6 must be joined together and preferably form part of a ground plane. The Signal Ground must also be connected to the ±8 V power supply ground. The potential of the Logic Ground (LG) pin 9 can deviate from the Signal Ground by ±0.5 V maximum. Alternatively, the signal and logic grounds can be joined together at one point only.

An external load current of 2 to 8 mA should be supplied from each output bus to negative supply. For most applications a load resistor of 1.21 kΩ, 1% is recommended to minimize offset drift with temperature. In order to improve differential phase and tighten the insertion loss tolerance, an external constant current active load may be substituted for the load resistor. Note however, that since only one GX214 output drives the output bus at any one time, only one external load is needed for the bus.

A typical application is shown below. Two GX214 ICs are paralleled to form an 8x1 crosspoint matrix. The three address lines make use of the A0, A1 and $\overline{CS}$ inputs. If more than two devices are used in parallel, a decoder is necessary in order to generate the extra address inputs.

Depending on the application and the speed of the logic family used, latches may be required for synchronization where timing delays are critical. The active switching circuitry of the GX214 ensures low crosstalk and high performance over an input voltage range of -1.2 to +5.0 volts.



8x1 Video Multiplexer Incorporating Two GX214 Devices

GENNUM CORPORATION

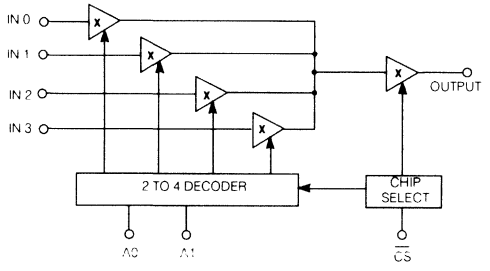
Wideband, Monolithic 4x1 Video Crosspoint Switches

GX4304, GX4314, GX4324, GX4334 TENTATIVE DATA SHEET

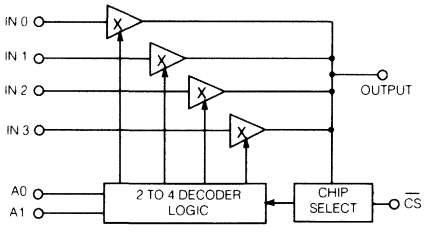
FEATURES

- low differential phase and gain
- wide bandwidth, 300 MHz at -3 dB
- small switching transient
- ±4.5 to ±13.2 volts supplies
- low and high power versions

FUNCTIONAL BLOCK DIAGRAMS



High Power
GX4304, GX4314



Low Power
GX4324, GX4334

TRUTH TABLE

ALL VERSIONS

$\overline{CS}$	A1	A0	OUTPUT
0	0	0	IN 0
0	0	1	IN 1
0	1	0	IN 2
0	1	1	IN 3
1	X	X	HI - Z

X = DON'T CARE

CIRCUIT DESCRIPTION

The GX4304, GX4314, GX4324 and GX4334 are wideband video multiplexers implemented in bipolar technology. These devices are characterized by excellent differential phase and gain in the enabled state, very high off-isolation in the disabled state and fully buffered unilateral signal path. Make-before-break switching assures virtually glitch-free switching.

For use in NxM routing matrices, these devices feature a very high, nearly constant input impedance coupled with high output impedance in the disabled state. This allows multiple devices to be paralleled at the inputs and outputs without additional circuitry.

Logic inputs are TTL and 5V CMOS compatible, providing address and chip select functions. The operation of the devices is described in the Truth Table below.

The GX4304 and GX4314 require an additional 8 mA of supply current over the low power versions.

In addition, the GX4304 and GX4324 require an external 1% resistor connected between pin 9 and Ground, in order to tightly control signal delay matching from chip to chip. The GX4314 and GX4334 have an on-chip lower tolerance resistor for this function. Table 1 highlights the various device configurations.

All these devices are members of the wideband video crosspoint family utilizing Gennum's proprietary LSI process.

The wideband GX4304 is pin for pin compatible with the high performance GX434, extending the flat frequency response characteristics from 50 to 100 MHz. Similarly, the GX4314 can replace the GX414 in order to extend the system frequency response.

APPLICATIONS

- HDTV
- Very high quality video switching
- Very high density video switching
- Computer graphics
- PCM / data routing

TABLE 1

POWER	EXTERNAL R	INTERNAL R
HIGH	GX4304	GX4314
LOW	GX4324	GX4334

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

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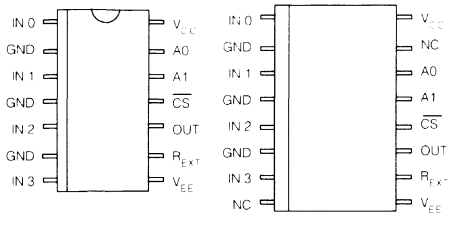
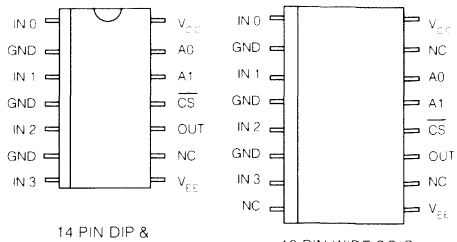
PIN CONNECTIONS



14 PIN DIP & 14 PIN NARROW SOIC GX4304 GX4324

16 PIN WIDE SOIC



14 PIN DIP & 14 PIN NARROW SOIC GX4314 GX4334

16 PIN WIDE SOIC

ELECTRICAL CHARACTERISTICS

(V_S = ±8V DC, 0°C ≤ T_A ≤ 70°C, R_L = 10kΩ, C_L = 30 pF, unless otherwise shown.)

	PARAMETER	SYMBOL	CONDITIONS	GX4304/14 MIN	GX4304/14 TYP	GX4304/14 MAX	GX4324/34 MIN	GX4324/34 TYP	GX4324/34 MAX	UNITS
DC SUPPLY	Supply Voltage	$\pm V_S$	Operating Range	±4.5	-	±13.2	±4.5	-	±13.2	V
	Supply Current	I^+	$\overline{CS}$ = 0	-	20	-	-	12	-	mA
		I^-	$\overline{CS}$ = 0	-	17	-	-	10	-	mA
		I^+	$\overline{CS}$ = 1	-	270	-	-	270	-	µA
		I^-	$\overline{CS}$ = 1	-	250	-	-	250	-	µA
STATIC	Analog Output Voltage Swing	V_{OUT}	Extremes before clipping occurs	-2.4	-	3	-2.4	-	3.6	V
	Analog Input Bias Current	I_{BIAS}		-	5	-	-	5	-	µA
	Output Offset Voltage	V_{OS}	T_A = 25°C	-7	-	7	-7	-	7	mV
	Output Offset Voltage Drift	ΔV_{OS}		-	15	60	-	15	60	µV/°C
LOGIC	Chip Enable Time	t_{ON}	Enable input to appearance of signal	-	350	500	-	350	500	ns
	Chip Disable Time	t_{OFF}	Enable input to disappearance of signal at output	0.6	1.0	-	0.6	1.0	-	µs
	Logic Input Thresholds	V_{IH}	1	2.0	-	-	2.0	-	-	V
		V_{IL}	0	-	-	0.8	-	-	0.8	V
	Logic Input Current	I_L		-	-	4	-	-	4	µA
DYNAMIC	Insertion Loss	I.L.	1V p-p sine or sq. wave at 100 kHz	-	0.03	-	-	0.03	-	dB
	Bandwidth (-3dB)	B.W.	small signal C_L = 0 pF	-	300	-	-	200	-	MHz
	Input Resistance	R_{IN}	$\overline{CS}$ = 0, crosspoint on	1.0	-	-	1.0	-	-	MΩ
	Input Capacitance	C_{IN}	$\overline{CS}$ = 0, crosspoint on	-	1.5	-	-	1.5	-	pF
	Output Resistance	R_{OUT}	$\overline{CS}$ = 0, crosspoint on	-	7	-	-	18	-	Ω
	Output Capacitance	C_{OUT}	$\overline{CS}$ = 1, chip disabled	-	-	4	-	-	8	pF
	Differential Gain	dg	f = 3.58 MHz	-	-	0.03	-	-	0.03	%
	Differential Phase	dp	V_{IN} = 40 IRE	-	-	0.02	-	-	0.02	deg
	All Hostile Crosstalk	$XTLK_{AH}$	1Vp-p on 3 inputs 4 th input has 10Ω resistor to gnd f=30 MHz	80	-	-	80	-	-	dB
	Chip Disabled Crosstalk	$XTLK_{CD}$	Enabled device on O/P f=100 MHz	-	80	-	-	80	-	dB
	Slew Rate	+SR	V_{IN} = 3V p-p (C_L = 0 pF)	250	-	-	150	-	-	V/µs
		-SR	V_{IN} = 3V p-p (C_L = 0 pF)	250	-	-	150	-	-	V/µs

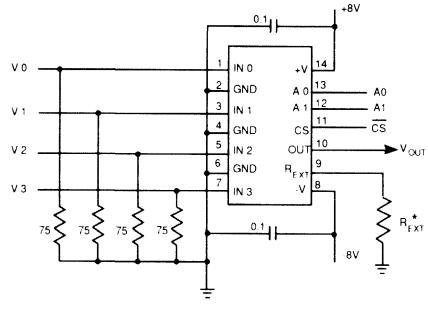
ELECTRICAL CHARACTERISTICS continued

DEVICE		CONDITIONS	MAX GAIN SPREAD (dB) f = 30 MHz	MAX XPT SCATTER (deg) R_S = 75Ω f = 3.58 MHz	
				25 °C	0 - 70 °C
High Power	GX4304	R_{EXT} = 33 kΩ from pin 9 to GND	±0.1	±0.1	±0.2
	GX4314		±0.2	±0.2	±0.4
Low Power	GX4324	R_{EXT} = 33 kΩ from pin 9 to GND	±0.2	±0.2	±0.4
	GX4334		±0.4	±0.4	±0.8

ABSOLUTE MAXIMUM RATINGS

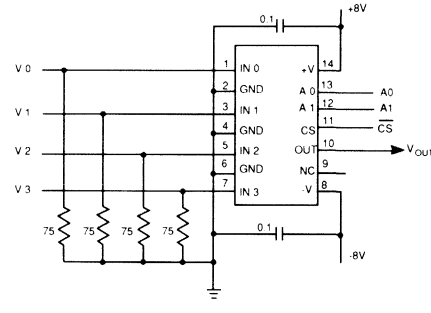
Parameter	Value
Supply Voltage	±13.5V
Operating Temperature Range	0°C ≤ T_A ≤ 70° C
Storage Temperature Range	-65°C ≤ T_S ≤ 150° C
Lead Temperature (Soldering, 10 Sec)	260° C
Analog Input Voltage	the greater of (V_{CC} - 14.3V) or V_{ff} the lesser of (15.8 V + V_{ff}) or V_{CC}
Logic Input Voltage	-0.5V ≤ V_L ≤ +5.5V

APPLICATION CIRCUITS



GX4304 / GX4324

*R_{EXT} is nominally 33 kΩ. The power consumption of the device may be reduced by up to 3 times by increasing the value of R_{EXT} up to 100 kΩ. The bandwidth and slew rate will be reduced under this condition.



GX4314 / GX4334

GENNUM CORPORATION

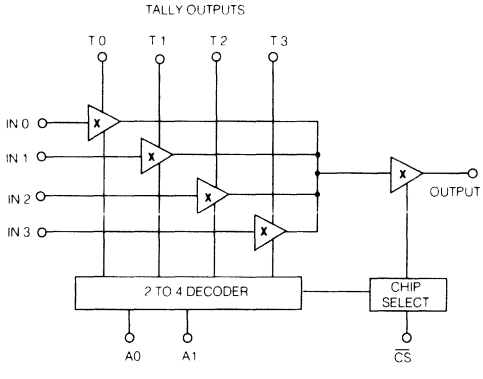
Wideband, Monolithic 4x1 Video Crosspoint Switches

GX4404, GX4414 TENTATIVE DATA SHEET

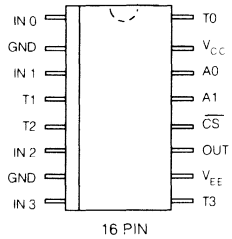
FEATURES

- low differential phase and gain
- wide bandwidth, 300 MHz at -3 dB
- small switching transient
- ±4.5 to ±13.2 volts supplies
- individual TALLY outputs
- low and high power versions

FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS



16 PIN
'NARROW' SOIC
(& 16 PIN DIP)

CIRCUIT DESCRIPTION

The GX4404 and GX4414 are wideband video multiplexers implemented in bipolar technology. These devices are characterized by excellent differential phase and gain in the enabled state, very high off-isolation in the disabled state. Fully buffered unilateral signal paths ensuring negligible output to input feedback, while delivering minimal output switching transients through make-before-break switching.

For use in NxM routing matrices, these devices feature a very high, nearly constant input impedance coupled with high output impedance in the disabled state. This allows multiple devices to be paralleled at the inputs and outputs without additional circuitry.

The chip is disabled when a logic HIGH is applied to the $\overline{CS}$ control pin. In this case, regardless of the ADDRESS data, the output of the device assumes a high impedance state.

Individual PNP to V_{CC} TALLY outputs provide positive indication of crosspoint selection. The GX4414 is a lower power version of the GX4404 and both are functionally identical.

All logic inputs are TTL and 5V CMOS compatible. Supply voltages can be between ±4.5 to ±13.2 volts.

These devices are members of the wideband video crosspoint family utilizing Gennum's proprietary LSI process.

APPLICATIONS

- HDTV
- Very high quality video switching
- Very high density video switching
- Computer graphics
- PCM / data routing matrices

TRUTH TABLE

				TALLY O/Ps			
$\overline{CS}$	A1	A0	OUT	T0	T1	T2	T3
0	0	0	IN 0	ON	*	*	*
0	0	1	IN 1	*	ON	*	*
0	1	0	IN 2	*	*	ON	*
0	1	1	IN 3	*	*	*	ON
1	X	X	HI - Z	*	*	*	*

X = DON'T CARE * = OFF (high impedance)

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ABSOLUTE MAXIMUM RATINGS

Parameter	Value
Supply Voltage	±13.5V
Operating Temperature Range	$0°C \le T_A \le 70°C$
Storage Temperature Range	$-65°C \le T_S \le 150°C$
Lead Temperature (Soldering, 10 Sec)	260° C

Parameter	Value
Analog Input Voltage	the greater of $(V_{CC} - 14.3V)$ or V_{EE} the lesser of $(15.8\ V + V_{EE})$ or V_{CC}
Logic Input Voltage	$-0.5V \le V_L \le +5.5V$
TALLY Output Current	2 mA

ELECTRICAL CHARACTERISTICS

(V_S = ±8V DC, $0°C \le T_A \le 70°C$, R_L = 10kΩ, C_L = 30 pF, unless otherwise shown.)

	PARAMETER	SYMBOL	CONDITIONS	GX4404 MIN	GX4404 TYP	GX4404 MAX	GX4414 MIN	GX4414 TYP	GX4414 MAX	UNITS
DC SUPPLY	Supply Voltage	$\pm V_S$	Operating Range	±4.5	-	±13.2	±4.5	-	±13.2	V
	Supply Current	I^+	$\overline{CS}$ = 0	-	20	-	-	12	-	mA
		I^-	$\overline{CS}$ = 0	-	17	-	-	10	-	mA
		I^+	$\overline{CS}$ = 1	-	270	-	-	270	-	µA
		I^-	$\overline{CS}$ = 1	-	250	-	-	250	-	µA
STATIC	Analog Output Voltage Swing	V_{OUT}	Extremes before clipping occurs	-2.4	-	3	-2.4	-	3.6	V
	Analog Input Bias Current	I_{BIAS}		-	5	-	-	5	-	µA
	Output Offset Voltage	V_{OS}	T_A = 25°C	-7	-	7	-7	-	7	mV
	Output Offset Voltage Drift	ΔV_{OS}		-	15	60	-	15	60	µV/°C
LOGIC	Chip Enable Time	t_{ON}	Enable input to appearance of signal	-	350	500	-	350	500	ns
	Chip Disable Time	t_{OFF}	Enable input to disappearance of signal at output.	0.6	1.0	-	0.6	1.0	-	µs
	Logic Input Thresholds	V_{IH}	1	2.0	-	-	2.0	-	-	V
		V_{IL}	0	-	-	0.8	-	-	0.8	V
	Logic Input Current	I_L		-	-	4	-	-	4	µA
	TALLY Outputs		$(V_{CC} - V_{TALLY})$ I_{TALLY} = 1mA	100	200	400	100	200	400	mV
DYNAMIC	Insertion Loss	I.L.	1V p-p sine or sq. wave at 100 kHz	-	0.03	-	-	0.03	-	dB
	Bandwidth (-3dB)	B.W.	small signal C_L = 0 pF	-	300	-	-	200	-	MHz
	Input Resistance	R_{IN}	$\overline{CS}$ = 0, crosspoint on	1.0	-	-	1.0	-	-	MΩ
	Input Capacitance	C_{IN}	$\overline{CS}$ = 0, crosspoint on	-	1.5	-	-	1.5	-	pF
	Output Resistance	R_{OUT}	$\overline{CS}$ = 0, crosspoint on	-	7	-	-	18	-	Ω
	Output Capacitance	C_{OUT}	$\overline{CS}$ = 1, chip disabled	-	-	4	-	-	8	pF
	Differential Gain	dg	f = 3.58 MHz	-	-	0.03	-	-	0.03	%
	Differential Phase	dp	V_{IN} = 40 IRE	-	-	0.02	-	-	0.02	deg
	All Hostile Crosstalk	$XTLK_{AH}$	1Vp-p on 3 inputs 4 th input has 10Ω resistor to gnd f=30 MHz	80	-	-	80	-	-	dB
	Chip Disabled Crosstalk	$XTLK_{CD}$	Enabled device on O/P f=100 MHz	-	80	-	-	80	-	dB
	Slew Rate	+SR	V_{IN} = 3V p-p (C_L = 0 pF)	250	-	-	150	-	-	V/µs
		-SR	V_{IN} = 3V p-p (C_L = 0 pF)	250	-	-	150	-	-	V/µs
	Gain Spread at 30 MHz	ΔA_V		-	-	±0.2	-	-	±0.4	dB
	Crosspoint Scatter		R_S = 75Ω, T_A = 25°C	-	-	±0.2	-	-	±0.4	deg
			f = 3.58 MHz, 0°C < T_A < 70°C	-	-	±0.4	-	-	±0.8	deg

GENNUM CORPORATION

HDTV 8x1 and 10x1 Modular Video Multiplexers

GM8108/GM8110 ADVANCE INFORMATION NOTE

FEATURES

- ±4.5 to ±5.5 volts supplies
- wide bandwidth, 300 MHz at -3 dB
- less than 0.04% differential gain at 4.5 MHz
- less than 0.02° differential phase at 4.5 MHz
- greater than 70 dB all hostile crosstalk at 10 MHz
- greater than 70 dB off-isolation at 30 MHz
- expandable

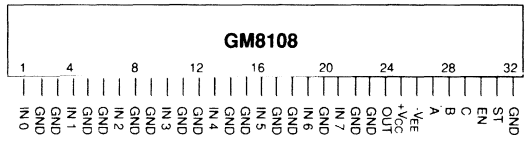
GM8108 8x1 Multiplexer Module

GM8108 — CIRCUIT DESCRIPTION

The Gennum GM8108 Multiplexer module uses eight GX4201 wideband crosspoints configured as an 8x1 HDTV video multiplexer. On-board decoding and latching combined with tri-state outputs and extremely high input impedance allows for simple multiplexer expansion.

The on-board logic uses a negative STROBE to latch the address data. The latching occurs when the STROBE line returns to a high logic level. A separate ENABLE input controls crosspoint selection and is active low. When the ENABLE line is high, all eight crosspoint switches are off.

The circuit is packaged on a miniature printed circuit board (3.2in.x 0.5in.) having 32 pins spaced at 0.1in. arranged along one side. This SIP configuration means that routing of inputs, outputs and control lines is straightforward and convenient. Power supply requirements are ±5 volts and the module draws an average of 19 mA when enabled and only 3.5 mA when disabled.



GM8110 — CIRCUIT DESCRIPTION

The Gennum GM8110 Multiplexer module uses ten GX4201 wideband crosspoints configured as a 10x1 HDTV video multiplexer. On-board decoding combined with tri-state outputs and extremely high input impedance allows for simple multiplexer expansion.

The circuit is packaged on a miniature printed circuit board (4.0" x 0.55") having 40 pins spaced at 0.1" arranged along one side. This SIP configuration means that routing of inputs, outputs and control lines is straightforward and convenient. Power supply requirements are ±5 volts and the module draws an average of 20 mA when enabled and only 3.6 mA when disabled.

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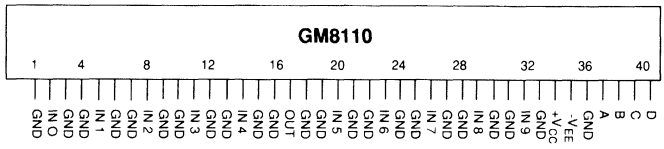

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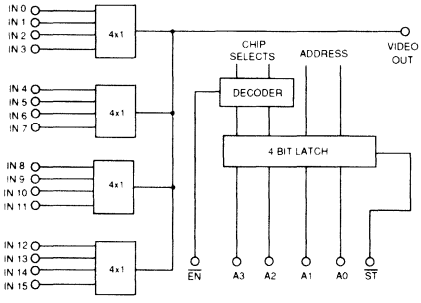
16x1 Video Multiplexer Modules

GM8116, GM8216, GM8316, GM8416 TENTATIVE DATA SHEET

FEATURES

- **single 45 lead SIP**
- **on-board decoding and latching**
- **minimal external parts required**
- **convenient 16x1 configuration**
- **both broadcast and CCTV versions**
- **high density routing: over 5 crosspoints per sq. in.**

FUNCTIONAL SCHEMATIC - ALL VERSIONS



TRUTH TABLE

EN	ST	A3	A2	A1	A0	O/P
1	X	X	X	X	X	HI - Z
0	0	0	0	0	0	IN 0
0	0	0	0	0	1	IN 1
0	0	0	0	1	0	IN 2
0	0	0	0	1	1	IN 3
0	0	0	1	0	0	IN 4
0	0	0	1	0	1	IN 5
0	0	0	1	1	0	IN 6
0	0	0	1	1	1	IN 7
0	0	1	0	0	0	IN 8
0	0	1	0	0	1	IN 9
0	0	1	0	1	0	IN 10
0	0	1	0	1	1	IN 11
0	0	1	1	0	0	IN 12
0	0	1	1	0	1	IN 13
0	0	1	1	1	0	IN 14
0	0	1	1	1	1	IN 15
0	↓	X	X	X	X	latch state

X = don't care

CIRCUIT DESCRIPTION

These modules are designed as 16 x 1 video multiplexers for use in broadcast and CCTV routers and switchers. They use surface mount components made up of four 4x1 crosspoint devices, a monolithic decoder and a 4 bit latch all on one miniature board.

The wide versions use 300 mil SOIC crosspoint devices and are only 17.8 mm (0.7 in.) high. The narrow versions use 150 mil SOIC devices and are a mere 14.0 mm (0.55 in.) in height. The overall length of the module is only 116.8 mm (4.6 in.). These small dimensions mean that high density matrices can be made using several modules. Also, convenient SIP format pinouts make PCB layout of large N by M matrices simple and straightforward.

The entire module may be disabled by applying a logic ONE to the $\overline{\text{ENABLE}}$ input. Crosspoint selection is made by applying the correct address code to the address inputs and applying a logic ZERO to the $\overline{\text{STROBE}}$ input. Returning this level to logic ONE latches ON the crosspoints.

All logic inputs are TTL and 5 V CMOS compatible. The supply voltage range for the 8116 and 8216 modules are ±7 V to ±13.2V, and ±7 V to ±9.5 V for the 8316 and 8416 modules. Both require +5V for the logic circuits.

APPLICATIONS

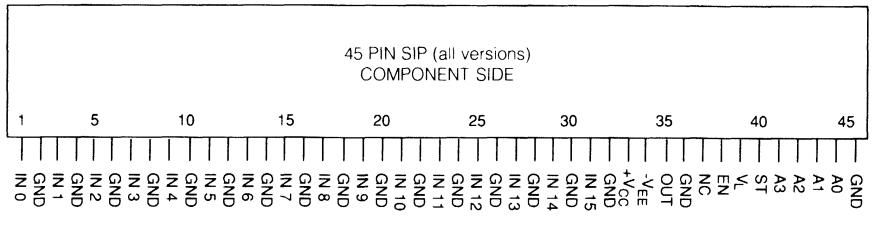
- Broadcast and CCTV video switching
- Building block for large video routers
- Very high density video matrices
- Stand alone 16x1 video multiplexers

Key for Pin Connections

IN	= video input	NC	= no connection
G	= ground	V_L	= logic supply voltage
V_{CC}	= positive supply voltage	EN	= enable
V_{EE}	= negative supply voltage	ST	= strobe
OUT	= video output	A	= address input

PIN CONNECTIONS

(ACTUAL SIZE — WIDE VERSION)



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ABSOLUTE MAXIMUM RATINGS

Parameter	Value
Power supply Voltage (GM8116/8216)	±13.5 V
Power supply Voltage (GM8116/8216)	±10.0 V
Logic supply voltage	+5.5 V
Analog input range (GM8116/8216)	$-4.0 \le V_S \le +2.4$ V
Analog input range (GM8116/8216)	$-4.0 \le V_S \le (V_{CC} + 0.3)$ V
Logic input voltage range	$0 \le V_L \le +5.5$ V
Operating temperature range	$0 \le T_A \le 70°C$
Storage temperature range	$-65 \le T_S \le 150°C$
Lead temperature (soldering 10 sec)	260°C

CONFIGURATIONS

Module	Module Width	Devices Used
GM8116	Wide	GX434 - - CKC
GM8216	Narrow	GX434 - - CKB
GM8316	Wide	GX214 - - CKC
GM8416	Narrow	GX214 - - CKB

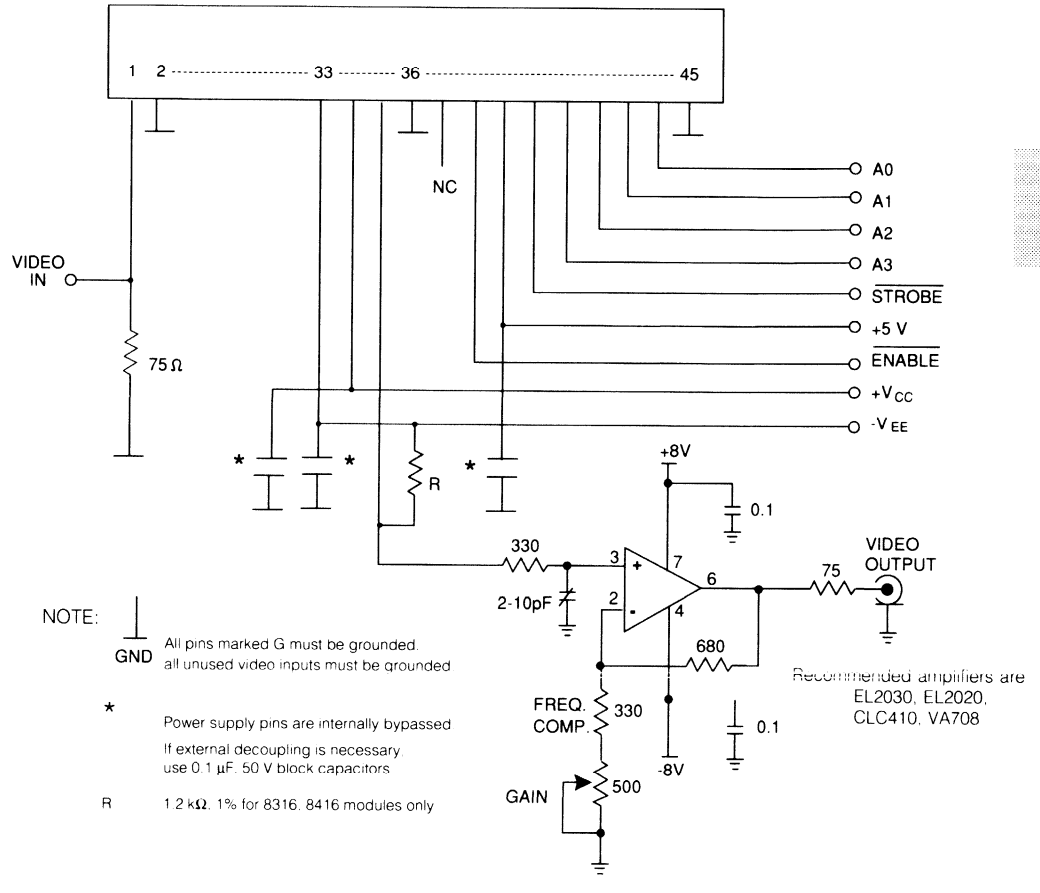
ELECTRICAL CHARACTERISTICS

($V_S = \pm 8$V DC, $0°C \le T_A \le 70°C$, $R_L = 10K$, $C_L = 0$ pF. [(ON) means **one** crosspoint on] unless otherwise shown.

			GM8116/8216			GM8316/8416			
PARAMETER	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Supply Voltage	$\pm V_S$		7	8	13.2	7.5	8	9.5	V
Supply Current	I^+	$\overline{Enable}$ = 0 (ON) $\overline{Enable}$ = 1 (OFF)	- -	11.7 1.8	13.3 2.4	- -	16 2.5	23 4	mA mA
	I^-	$\overline{Enable}$ = 0 (ON) $\overline{Enable}$ = 1 (OFF)	- -	11.0 1.2	12.5 1.6	- -	15 2.4	21 3.6	mA mA
Analog Output Voltage Swing	V_{OUT}	Extremes before clipping occurs	- -	- -	+2.0 -1.2	- -	- -	+5 -1.2	V V
Output Offset Voltage	V_{OS}	$T_A = 25°C$ 75Ω on each input to ground	0	7	14	-45	-80	-120	mV
XPT Turn-On Time	t_{ON}	Control input to appearance of signal	130	200	270	700	900	1100	ns
XPT Turn-Off Time	t_{OFF}	Control input to disappear. of signal	390	600	800	1200	2000	3000	ns
Insertion Loss	I.L.	1 V p-p at 100 kHz	0.025	0.03	0.04	0.1	0.13	0.16	dB
Bandwidth (-3dB)	B.W.	(see Note 1)	60	70	-	65	85	-	MHz
Input Resistance	R_{IN}	$\overline{Enable}$ = 0 (ON)	900	-	-	900	-	-	kΩ
Input Capacitance	C_{IN}	$\overline{Enable}$ = 0 (ON) $\overline{Enable}$ = 1 (OFF)	- -	2.0 2.4	- -	- -	2.0 2.2	- -	pF pF
Output Resistance	R_{OUT}	$\overline{Enable}$ = 0 (ON)	-	14	-	-	9	-	Ω
Output Capacitance	C_{OUT}	$\overline{Enable}$ = 1 (OFF)	-	60	-	-	48	-	pF
Differential Gain	dg	at colourburst 40 IRE	-	0.03	0.05	-	-	0.05	%
Differential Phase	dp	at colourburst 40 IRE	-	0.03	0.04	-	0.03	0.05	degrees
Crosstalk (all hostile)	$XTALK_{AH}$	f = 10 MHz (Note 2)	70	75	-	70	75	-	dB
Off-Isolation	$XTALK_{CD}$	f = 10 MHz (Note 3)	90	95	-	85	90	-	dB

Note1: Frequency peaking of +6 to +8dB between 40 - 60 MHz on 8316/8416 modules. Frequency is flattened on the 8116/8216 modules and no peaking occurs
Note 2: Sweep on 15 inputs 1 V p-p, 16th input has 75Ω to ground
Note 3: Output is loaded with one enabled module whose ON input has a 37.5Ω resistor to ground

TYPICAL APPLICATION CIRCUIT



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GENNUM CORPORATION

Measuring Up To Broadcast (Differential Gain and Phase)

by John Francis and Paul Moore, Design Engineers, Video/Broadcast Products

INFORMATION NOTE

INTRODUCTION

Measuring non-linearities in video switching systems can be a demanding task when using standard test signal and oscillographic techniques. While it may be possible to measure the relatively large system distortions in this manner, measurement of differential gain (dg) and differential phase (dp) in the smallest system component, the video switch IC, calls for more precise and accurate methods.

In creating a line of video switch products, we have found it necessary to develop improved resolution dg and dp measurement techniques which yield better than 0.001% and 0.001 degrees accuracy. This measurement expertise allows us to minimize crosspoint distortion through optimization of circuit design and application methodology

THE TEST SIGNAL

IEEE Std 206 defines differential gain and phase as the change in magnitude and phase of a small amplitude, high frequency sine wave summed with a low frequency signal changing between two stated levels. As it relates to a composite color television system, differential gain and phase are measured for 20 IRE units of color subcarrier superimposed on a luminance signal which varies from blanking level (0 IRE) to white level (100 IRE).

For AC coupled systems, the average picture level (APL) should be maintained at 10%, 50%, or 90% to ensure that the full range of average operating conditions are observed. Also, a time-varying luminance signal of near 15kHz is usually used as the low frequency component.

For DC coupled systems, the APL does not affect the operating point of the circuit under test and hence is not significant. Further, a well-defined DC luminance component can be used if it is assumed that the DC response of the crosspoint is equivalent to its low frequency response. This is a valid assumption for the wideband video crosspoint. DC conditions simplify the measurement while allowing the use of high resolution test equipment.

To simulate the operating conditions of an AC coupled, composite video system while making a DC coupled measurement, the following table may be used. It shows the required blanking and luminance levels of the test signal for 10%, 50%, and 90% APL in steps of 12.5 IRE units per IEEE Std 206.

DC Coupled		AC Coupled					
APL irrelevant		10% APL		50% APL		90% APL	
Blanking Level (V)	Luminance Level (V)	Blanking Level (V)	Luminance Level (V)	Blanking Level (V)	Luminance Level (V)	Blanking Level (V)	Luminance Level (V)
0	.089	-.029	.060	-.250	-.161	-.464	-.375
0	.179	-.029	.150	-.250	-.071	-.464	-.286
0	.268	-.029	.239	-.250	.018	-.464	-.196
0	.357	-.029	.328	-.250	.107	-.464	-.107
0	.446	-.029	.417	-.250	.196	-.464	-.018
0	.536	-.029	.507	-.250	.286	-.464	.072
0	.625	-.029	.596	-.250	.375	-.464	.161
0	.714	-.029	.685	-.250	.464	-.464	.250

where white level = 100 IRE = 0.714 V (when DC coupled)

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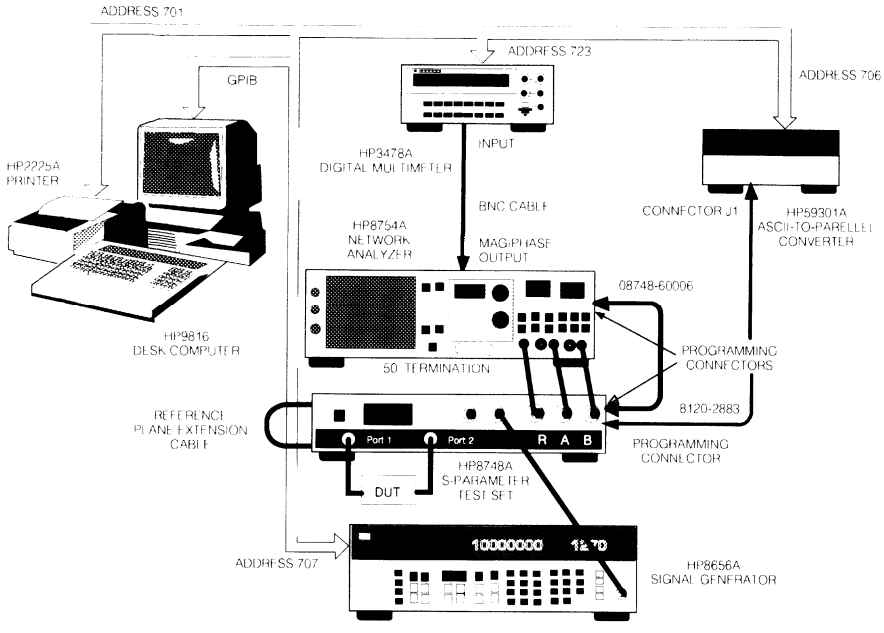

Fig.1 System Block Diagram

MEASUREMENT METHOD

The test equipment used to measure dg and dp is shown in Figure 1.
It consists of :

HP8754A	Network Analyzer
HP 8748A	S-parameter Test Set
HP8656A	Signal Generator
HP3478A	Digital Multimeter
HP59301A	ASCII-to-Parallel Converter
HP9816	Computer
HP2225A	Think Jet Printer

The signal generator is programmed to provide a stable and accurate color subcarrier of user-definable frequency and amplitude. This reference signal is applied to the input of the S-parameter test set and thereby to the device under test (DUT) through port 1 (signal R). The output from the DUT is sampled at port 2 of the S-parameter test set (signal B). The forward transfer characteristic (S21 = B/R) is passed to the network analyzer where the magnitude and phase are measured. A DVM allows the 9816 computer to read the measurement over the General Purpose Interface Bus (GPIB).

As shown in Figure 2, software running on the 9816 computer leads the user through the measurement routine while controlling the test equipment over the GPIB. The computer prompts the user to specify:-

a) gain or phase measurement
b) frequency and amplitude of the subcarrier, and
c) blanking and luminance levels.

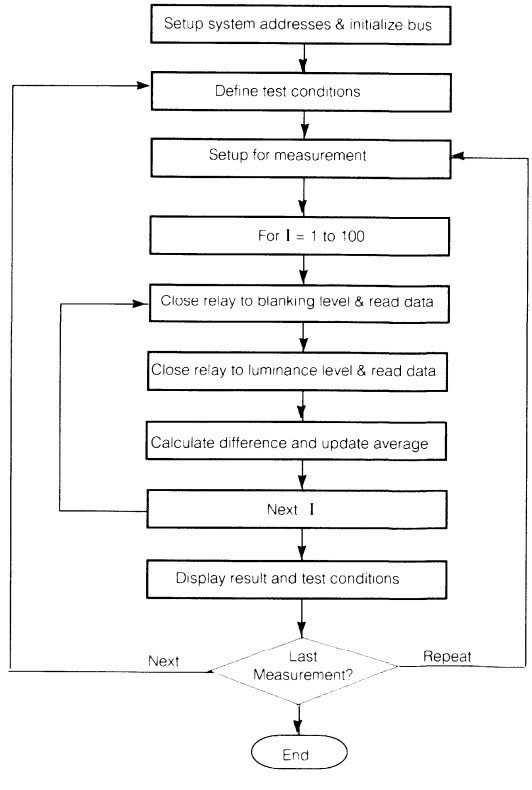

Fig. 2 Flow Chart of Differential Gain and Phase Measurement Program.

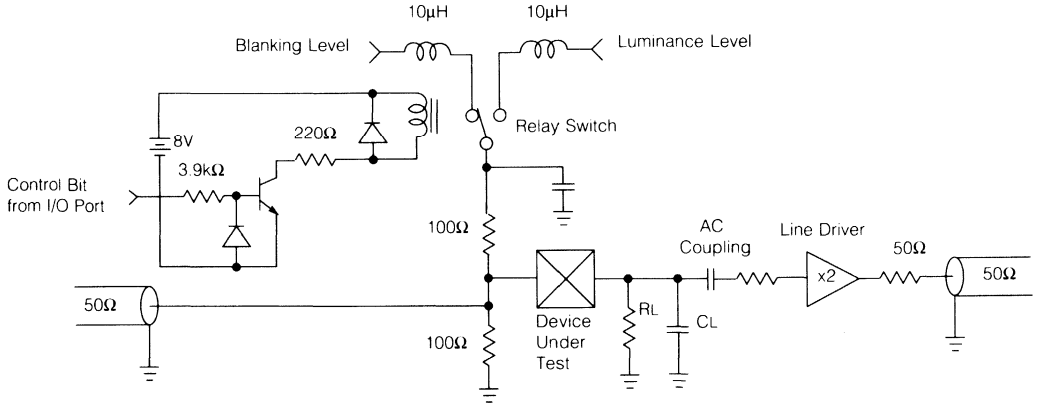

Fig. 3 Simplified Test Circuit

The test circuit of Figure 3 allows two DC bias levels, set by the user, to be superimposed on the color subcarrier from port 1 of the S-parameter test set. A relay,controlled by the 9816 computer, selects either the preset blanking or luminance level. The program takes one measurement at each level and calculates the change in gain or phase of S21. This procedure is repeated one hundred times to provide a reasonably large sample. The results are averaged to reduce the standard deviation and therefore improve the accuracy of the measurement.

The output from the device under test is AC coupled to a buffer amplifier which drives the 50Ω line to port 2 of the S-parameter test set. AC coupling allows the buffer to operate at a constant luminance level so that it does not contribute any dg or dp to the measurement.

MEASUREMENT ACCURACY

The accuracy of the measurement is dependant on :

a) the constancy of the subcarrier signal
b) noise
c) temperature drift.

Since dg and dp are relative measurements, the absolute gain and phase of the forward transfer characteristic (S21) are irrelevant. However, any change in gain or phase not resulting from a change in the luminance level constitutes an error.

Two methods can be used to assess the accuracy of dg / dp measurements:

In the first method, a shorting link is connected in place of the device under test. A typical measurement of dg and dp for this configuration is 0.0002% and 0.0006 degrees. The change in source impedance between coupling the blanking and luminance levels to the input contributes most of this error.

In the second, disconnecting the control to the relay places the device under test at a constant DC bias. Measurements performed on this configuration should give zero dg and dp; in fact, the results are less than 0.0001% for dg and 0.0001 degrees for dp.

These checks ensure that:

a) error from noise is made insignificant by averaging the measurements
b) drift problems do not contribute significant errors.

The important result of this exercise is that the typical GX414 data sheet specifications for dg and dp of 0.03% and 0.012 degrees are not our imagination but can be verified through measurement!

Virtually *Glitch-free* Bipolar Crosspoint Switches

by J. Ian Ridpath and Paul Moore, Design Engineers, Video & Broadcast Products

INFORMATION NOTE

INTRODUCTION

Bipolar video crosspoint switches manufactured by Gennum Corporation are virtually *glitch-free* when compared to switches using CMOS and DMOS technologies.

The reason?

Gennum designed a make-before-break switching circuit to keep the output switching transients small. In addition, the bipolar, unidirectional transmission path offers extremely high output to input signal isolation.

MOS BREAK-BEFORE-MAKE SWITCHING

Both CMOS and DMOS switching are accomplished by altering the channel resistance of the switching transistors from a high impedance off-state to a low impedance on-state. The on-state, (whether or not the switch is configured as a 'T') allows bidirectional transmission of signals from the input to output as well as output to input.

When switching to a second channel, a dead-time must be incorporated to ensure that both channels are not on at the same time. If they are, the two inputs would be effectively shorted together by the on-channel resistances. This break-before-make switching action causes severe *glitches* on the output which are in part coupled to the input by the bidirectional transmission path.

BIPOLAR MAKE-BEFORE-BREAK SWITCHING

In bipolar crosspoints, the output to the input isolation in the enabled or on-state is typically in excess of 85 dB. A series of emitter followers and level shifting diodes produce a transmission path which is inherently unidirectional. Turning on two crosspoints at once results in the signals mixing at the output but interferes little with the input signals. This allows the use of make-before-break switching which keeps the output transient very small.

COMPARISON OF TRANSIENTS BETWEEN CMOS, DMOS AND BIPOLAR SWITCHES

The test set-up to compare the switching transients of a buffered MOS, a T-configured MOS and Gennum's bipolar GX414 monolithic crosspoint is shown in Figure 1.

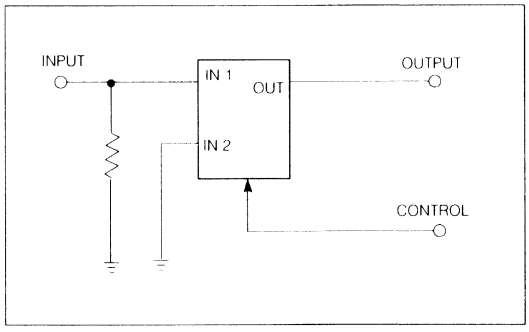

Figure 1

The signal causes the switches to alternate between Input 1 and Input 2. IN 1 is tied to ground by a 75 Ω resistor so that the voltage on it can be monitored by an oscilloscope, while IN 2 is tied directly to ground.

Figures 2, 3 and 4 show the results of these tests. The left hand side of each of these figures show IN 1 and output waveforms when the switch is toggled from IN 1 to IN 2. The right hand side shows the same points when the switch is toggled back from IN 2 to IN 1.

In the buffered CMOS example of Figure 2, an output *glitch* appears which exceeds 250 mV in both the positive and negative direction and a reflected input *glitch* of approximately 10 mV. This output transient is reflected back to the input because the channel is still ON for a short period of time. When switching back from IN 2 to IN 1 the input *glitch* is smaller, since the channel from IN 1 to the output is not yet made. The duration of the input *glitch* is approximately 20 ns, while the output transient rings for an additional 100 ns.

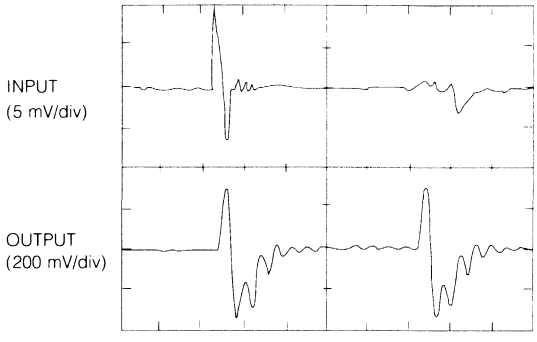

Fig. 2 T-Buffered CMOS (50 ns/div)

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Figure 3 shows that under similar switching conditions, the T-configured DMOS device has a large negative transient of over 100 mV at the input when switched from channel 1 to channel 2, and a smaller positive transient when the device is toggled back. The large negative pulse at the output represents the dead-time and clearly shows the break-before-make switching action. However, it should be noted that a large amount of overshoot occurs on the rising edge of the output signal. Again, the duration of the input *glitches* is quite short and varies between 20 ns to 40 ns, while the output dead-time exceeds 70 ns.

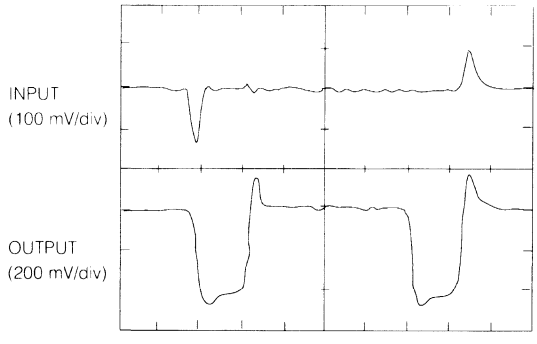

Fig. 3 T-Configured DMOS (50 ns/div)

The last figure shows the minimal transients produced by the bipolar crosspoint. Note the change in scales for both the amplitude and time duration. The input *glitches* are not due to the output transients, but are a function of the bias current on the input emitter follower transistor. The negative going output transient is less than 20 mV peak, and has a duration of approximately 100 ns. It is followed by a damped waveform of less than 20 mV peak, having a fundamental period of about 600 ns. These low frequency transients do not create any out-of-band noise and do not need to be filtered.

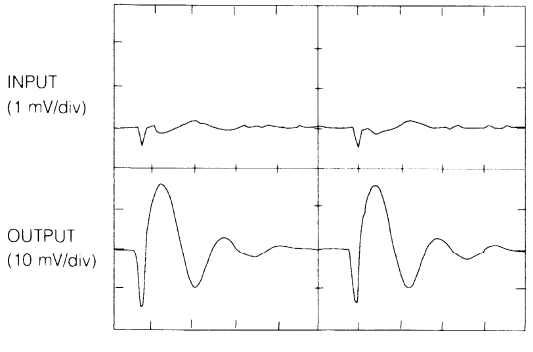

Fig.4 GX414 Bipolar (500 ns/div)

CONCLUSIONS

For MOS switches to be used as video crosspoints, extra external circuitry is always needed. The external circuitry usually consists of input buffers (having very low output impedance) and an output clamping circuit.

In DMOS circuits, the input buffer (which is usually an emitter follower) is used to provide isolation from the switching transients present at the input of each switch. If the buffer was not included and multi-inputs were used in a matrix configuration, *glitches* would appear on the input bus and affect all other crosspoints connected to that bus. Gennum's GX414, GX414A, GX424 and GX434 bipolar crosspoints have that buffer built-in.

The ratio of ON to OFF capacitance at the input of a MOS switch can be an order of magnitude or more. The absolute capacitance could change from 4 pF to 45 pF. This means the input drive signal sees an undesireable, widely changing impedance. With the built-in buffer the Gennum products listed have an input ON to OFF capacitance ratio near unity, with absolute values of only 2.0 pF and 2.4 pF.

The serious output *glitches* produced by the MOS switches could be interpreted as sync pulses by subsequent equipment. To remove this problem, the output must be clamped during the switching dead-time. The output transients generated by Gennum crosspoints are extremely small and clamping is not needed.

Even though MOS crosspoint switches consume less power, the saving is negated by the external circuitry necessary to make the switch function properly in a video system. Gennum's family of bipolar crosspoints require no extra circuitry since they are designed specifically for video routing and switching applications.

GENNUM CORPORATION

Comparison of 4x1 Video Crosspoint Switches

by Ian Ridpath, Senior Applications Engineer, Video/Broadcast Products

INFORMATION NOTE

A Look at Parameter and Operating Differences Between the GX414, GX414A, GX424 and GX434 Monolithic, Bipolar, 4x1 Video Crosspoint Switches

INTRODUCTION

It is perhaps worthwhile, before looking into the differences, to view the similarities between members of this family of high performance video crosspoint switches. Functionally, all the devices represent a 4x1 crosspoint configuration as shown in Figure 1.

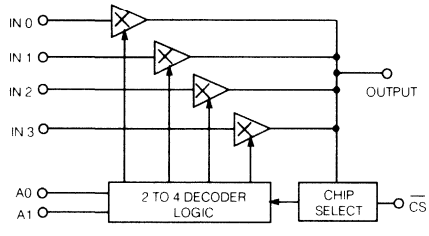

Fig. 1 Functional Diagram

They are all pin-for-pin compatible with the exception of the GX434 which uses the normally unused pin 9 as a connection point for an external 1% resistor. They are all available in standard 14 pin DIP and 16 pin SOIC packages.

The data sheets provide detailed electrical parameter specifications and performance graphs for each device. This information note looks specifically at the differences in some of the parameters, how they are achieved, and their effect on the selection of a member of this family group for a particular application.

DEVICE COMPARISONS

COMPARISON 1: GX424 vs GX414

The GX424 is identical in all operating respects to the GX414; only the *'test program'* varies for each device, in order to allow the GX424 to pass with wider parameter spreads and reduced specifications. These wider spreads and reduced specifications are compared in Table 1.

PARAMETER	UNITS	GX424	GX414
Maximum supply current	(mA)	18	14
Output offset voltage range	(mV)	-20 to +30	-2 to +12
Maximum offset drift	µV/°C	+300	+200
Input to output delay spread at 25°C (chip-to-chip)	(deg)	±0.80	±0.35
Address logic (turn-on time)	(ns)	100 to 350	130 to 270
Chip selection (turn-on time)	(ns)	150 to 450	200 to 400
Maximum differential gain	(%)	0.1	0.05
Maximum differential phase	(deg)	0.05	0.025
Max. insertion loss at 10 kHz	(dB)	0.06	0.05
Minimum 3 dB bandwidth (C_L = 30 pF)	(MHz)	80	90
Gain spread at 8 MHz (C_L = 30 pF)	(dB)	+0.46 -0.12	±0.1
Min. OFF isolation at 10 MHz	(dB)	90	100
Min. all hostile crosstalk at 5 MHz	(dB)	92	94
Minimum slew rate (C_L = 0 pF)	(V/µs)	+60 -50	+84 -70
Relative cost		lower	

Table 1

The video system designer has the choice of using either the GX414 or GX424 depending whether or not, for the sake of cost-effectiveness, a sacrifice in performance is warranted.

COMPARISON 2: GX414A vs GX414

Nearly all parameters are the same for the two devices. The exceptions are shown in Table 2. (see over)

An additional processing stage (on-chip capacitance) compensates for frequency peaking but reduces the slew rate.

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PARAMETER	UNITS	GX414A	GX414
Input to output signal delay matching (chip-to-chip)	(deg)	±0.6	±0.35
Gain spread at 8 MHz	(dB)	±0.25	±0.1
Typical slew rate (C_L = 0 pF)	(V/µs)	±40	+120 -100
Relative cost		higher	

Table 2

COMPARISON 3: GX434 vs GX414

The parameters and operating characteristics of the GX434 most closely resemble the GX414. The normally unused pin 9 is now employed for connecting an external precision resistor. The parameter differences between the two devices are tabulated in Table 3.

PARAMETER	UNITS	GX434	GX414
Input to output signal delay matching chip-to-chip			
at T_A = 25°C	(deg)	±0.15	±0.35
at Full temp range	(deg)	±0.3	±0.7
Max. supply current	(mA)	11.5	14
Min. 3 dB bandwidth (C_L = 30 pF)	(MHz)	100	90
Gain spread at 8 MHz	(dB)	+0.06 - 0.04	±0.1
Typical slew rate (C_L = 0 pF)	(V/µs)	+450 -200	+120 -100

Table 3

This higher degree of delay matching and gain spread is achieved by using an external 33.2 kΩ, 1% resistor connected to pin 9. All the other 4x1 devices compared in this note use an onboard resistor which has a tolerance of between 20 and 25 percent. These resistors effectively control currents within the chip that determine the input-to-output signal delay. The tighter the control of the resistor tolerance, the less is the chip-to-chip delay spread.

The difference in the frequency response values and slew rate are due to a modification to the on-chip frequency peaking compensation network.

CONCLUSIONS

Even though this particular group of devices is similar in so many respects, the differences described are significant to the video systems designer. This is especially true if a cost-effective yet performance enhanced system is required.

The design and application engineers at Gennum are always happy to discuss system requirements for any of the video crosspoint switch ICs.

Comparison of 16x1 Video Multiplexer

by J. Ian Ridpath, Senior Applications Engineer, Video & Broadcast Products

INFORMATION NOTE

INTRODUCTION

This document presents comparative technical information between the Gennum GX414 video crosspoint switches and the various DCMOS products offered by Siliconix Inc. as used in 16x1 video multiplexer. The 16x1 configuration was chosen because it is quite often a basic building block found in many production switchers and routing systems.

No direct cost comparison has been made since the final assembled cost of a PCB varies, depending on whether standard or surface mounting techniques are used. However, a parts list is included for each circuit in order to allow the design engineer to cost each system on its own. The only assumption that has been made is that the best cost-effective solution (with highest performance specifications) is desired by the video design engineer.

The four circuits presented, compare the Gennum GX414 internally buffered bipolar 4x1 crosspoint to the Siliconix 16x1, 8x1 and 4x1 circuits represented by their DG536, DG538 and DG540 DCMOS integrated circuits.

THE GENNUM GX414 SOLUTION

The desired 16x1 configuration is simply implemented using four GX414 video crosspoint integrated circuits along with some address decoding and latching. No input buffer stages are needed with this circuit. The features of the Gennum solution are:

- extremely low differential phase and gain*
- extremely high isolation *
- no external transistors or resistors required
- minimal PCB board space (approximately 2" x 5")
- virtually no switching *glitches*
- virtually constant input capacitance (2.0 pF to 2.4 pF maximum variation).

Parts List

4 - GX414 IC (switches)
10 - Supply rail bypass capacitors
1 - 74HC139 IC (chip select decoder)
1 - MC14042 IC (quad latch)
2 - 16 way connectors (video inputs and grounds)
1 - 10 way connector (address/ enable/ strobe/ power and video out)
1 - PCB approx. 2" x 5"
Total parts count = 20

* See Gennum Data Sheet 510-38

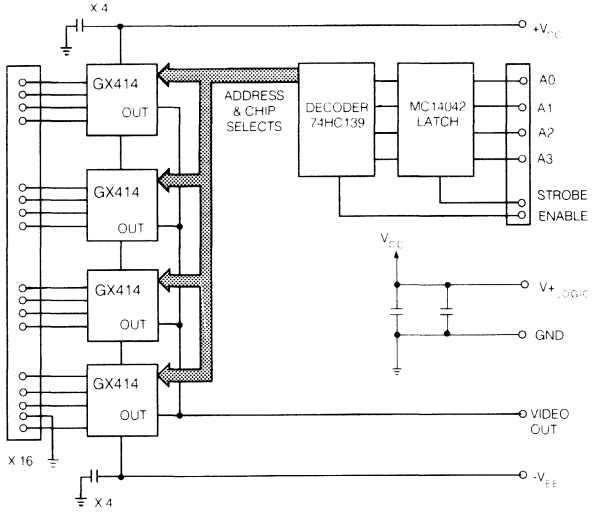

Fig. 1 Circuit Diagram of the 16x1 Multiplexer Using Four GX414 Devices

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THE SILICONIX DG-536 SOLUTION

This device has onboard address decoding and latching for all 16 switches. The logic inputs include Chip Select, Enable and Strobe, requiring virtually no external logic circuitry. When using split power supplies however, (for best differential phase and gain), the logic inputs must be level shifted.

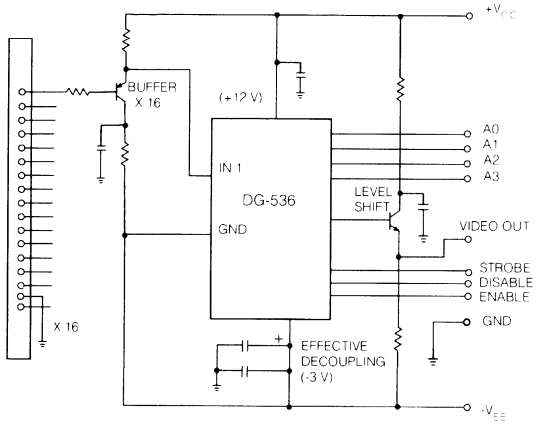

Fig. 2 Circuit Diagram of the DG-536 16x1 Multiplexer

The MOS bilateral channels require buffering at their inputs in order to prevent the flow of signal and switching transients from output to input. The buffers are also necessary in order to reduce the large capacitance change at the input of each switch from the ON to OFF condition of the channel.

A level shifting NPN transistor is also required at the output in order to restore the correct DC reference. It is usually necessary to clamp the output during switching. These transistors with their associated bias components and bypass capacitors take up more room than the integrated circuit itself resulting in a PCB of about 5 inches by 4 inches. The associated component cost, PCB area and manufacturing complexity does not make this arrangement as cost effective as the Gennum solution.

Parts List

1 - DG-536 IC (16 switches, decoder/latches etc.)
16 - PNP bipolar transistors (buffers)
1 - NPN bipolar transistor (output level shifter)
50 - Resistors for above transistors
20 - Supply bypass capacitors
2 - 16 way connectors (video inputs)
1 - 4 way connector (address)
1 - 6 way connector (power, video out, control)
1 - PCB - (5" by 4").

Total parts count = 93

THE SILICONIX DG-538 SOLUTION

This device is configured as an 8x1 analog switch having improved specifications over the DG-536. As with the DG-536, external input transistor buffers are required. Also, in order to make a 16x1 matrix, two DG-538 integrated circuits

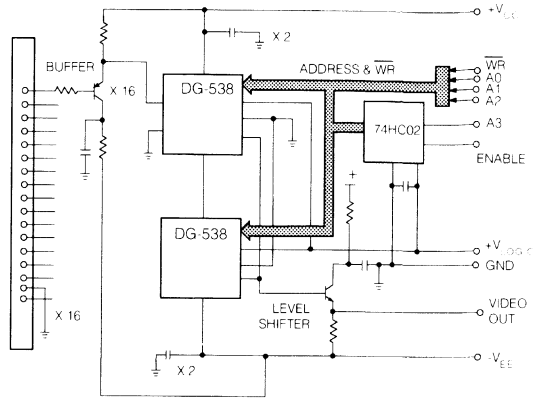

Fig. 3 Circuit Diagram of a DG-538 16x1 Multiplexer

are necessary. A small amount of external logic is required in order to select each device. This circuit uses address bit A3 as the controlling signal along with an ENABLE signal that disables the entire 16x1 multiplexer.

Parts list

2 - DG-538 IC (switches, decoder/latches)
1 - 74HC02 IC (A3 selection)
22 - Supply rail bypass capacitors
16 - PNP transistors (input buffers)
1 - NPN transistor (output level shifter)
50 - Resistors for the above transistors
2 - 16 way connectors (video inputs and grounds)
1 - 6 way connector (address, enable, video out)
1 - 4 way connector (power)
1 - PCB (4" x 5")

Total parts count = 97

THE SILICONIX DG-540 SOLUTION

The DG-540 is configured as four independent analog switches (quad SPST) and has improved frequency performance specifications over the DG-536 and DG-538 due to reduced capacitances and channel ON resistances.

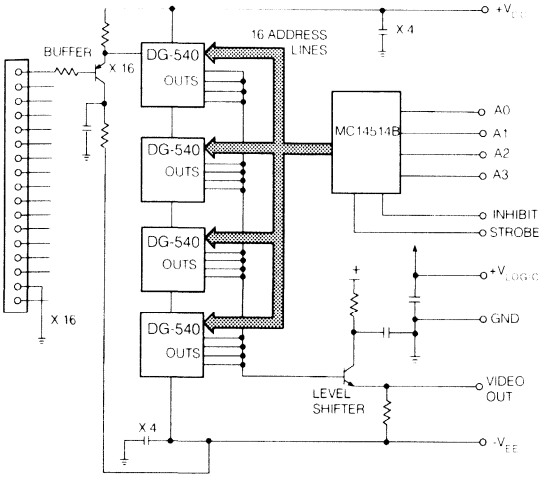

Fig. 4 Circuit Diagram of a DG-540 16x1 Multiplexer

As with the two other devices, the DG-540 requires input transistor buffers. Also, since the device is made up of independent switches with no address decoding nor chip enable function, these have to be provided by external logic. Fortunately, a single 4 to 16 encoder such as the Motorola MC14514B, will perform the Address Selection, Enable and Strobe functions. This device is a 24 pin DIP and occupies a fair amount of PCB real estate. This combined with the area needed for the sixteen input buffers, makes the size of the multiplexer board similar to that of the DG-536 and DG-538.

Parts list

4 - DG-540 IC (switches)
26 - Supply rail bypass capacitors
16 - Transistors (input buffers)
1 - NPN transistor (output level shifter)
50 - Resistors for the above transistors
1 - MC14514B IC (decoder/ latch)
2 - 16 way connectors (video inputs and grounds)
1 - 6 way connector (address/ video out/ enable)
1 - 4 way connector (power)
1 - PCB - (5" by 4")

Total parts count = 102

CONCLUSIONS

The Gennum GX414 is the only device described which is specifically designed for video crosspoint matrices. Furthermore, only the GX414 data sheets specify differential gain and phase, two extremely important video parameters.

The GX414 is the only crosspoint using bipolar switches having unidirectional signal paths and make-before-break switching. These features mean that switching transients are extremely small and that there is virtually no feedback of these onto the input bus. Thus, no external input buffer stages are needed. The bipolar low impedance signal path also means that for high impedance loads (such as the output buffer stage), insertion loss is typically less than 0.035 dB.

At first glance it may appear as though the more complex internal circuitry of the DCMOS devices would have a simpler design solution. However, on comparing system component counts for the four circuits, it is evident that this is not the case.

The following table highlights the significant advantage offered by the Gennum GX414 solution in designing a 16x1 video crosspoint multiplexer.

Solution	Component Count	PCB Area SQ. IN.	Power Consumption (MW)
GX414	20	10	186*
DG536	93	20	242‡
DG538	97	20	304*
DG540	102	20	313*

* V_{CC} = ±8V. V_{LOGIC} = 5 V. T_A = 25°C.
(one crosspoint selected. all buffers on I_L = 1 mA)
‡ V_{CC} = +12 V. V_{EE} = -3 V

Engineers at Gennum are always willing to assist the video design engineer in achieving a high performance, cost effective solution to their video routing and switching requirements.

Frequency Peaking Compensation of the GX414 and GX424

by J. Ian Ridpath, Senior Applications Engineer, Video/Broadcast Products

APPLICATION NOTE

INTRODUCTION

In video switching applications, the crosspoint switch must meet several critical specifications which include differential phase, differential gain and frequency response flatness. The GX4 family of crosspoint switches exceed broadcast requirements for the above specifications. For wide bandwidth and high bit rate data applications, the frequency/flatness performance of these devices can be easily extended using information in this application note. Information presented gives the system designer two methods of frequency compensating a system using the GX414 and GX424 Video Crosspoint Switches.

The first method uses a small value series resistor placed in the output of each device. The second method utilises the frequency roll-off characteristics of the external video buffer amplifier.

CHARACTERISTICS OF THE GX414 AND GX424

The GX414 and GX424 are bipolar video crosspoint switches configured as shown in Figure 1. Each analog switch has an emitter follower input, some level shifting and clamping circuits and an emitter follower output. The four switch outputs are tied together and brought out to one common pin. At frequencies above 1 MHz, the emitter follower switches naturally exhibit frequency response peaking.

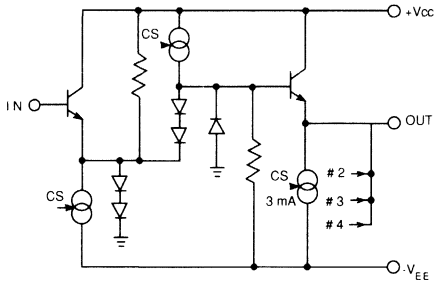

Fig.1 Enabled Crosspoint Equivalent Circuit

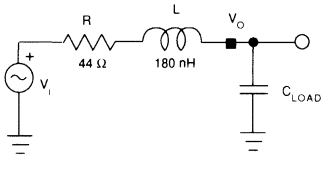

Fig.2 Output Impedance Model

The transfer function of this network is:

$$T_S = \frac{V_O}{V_I} = \frac{\frac{1}{LC}}{s^2 + s\left(\frac{R}{L}\right) + \frac{1}{LC}} \quad \ldots\ldots 1$$

This transfer function has a pair of complex conjugate poles with

$$f_O = \frac{1}{2\pi\sqrt{LC}} \quad \ldots\ldots 2$$

and

$$Q = \left(\frac{1}{R}\right)\left(\sqrt{\frac{L}{C}}\right) \quad \ldots\ldots 3$$

The frequency response peaks when $Q > 1/\sqrt{2}$ at a frequency equal to f_O, but it is maximally flat when $Q = 1/\sqrt{2}$.

In the above equations, the capacitance C, represents the load capacitor external to the device. With any value of C, a value of R can be found which will make $Q = 1/\sqrt{2}$, thus flattening the response. Practically, this can be accomplished by placing an external resistor in series with the output of the device.

In video routing or matrix switching applications, the load capacitance on the output bus is determined by how many devices are connected to the bus. A typical example as shown in Figure 3, uses five GX414s or five GX424s wired as a 20 x 1 matrix.

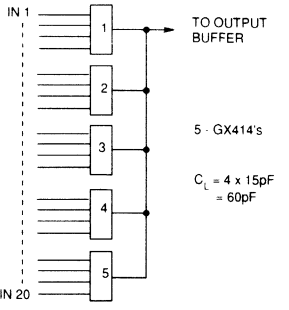

Fig.3 20 x 1 Matrix

For any single selected crosspoint, four of the devices will be disabled and one will be enabled (selected). The output capacitance of a disabled device is approximately 15 pF resulting in the total load capacitance seen by the selected device as approximately 60 pF. Assuming stray capacitance adds a further 5 pF to the system output, the total external capacitance will be approximately 65 pF.

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Method 1. Adding Series Resistance to the Output

Using equation 3), the value of R which will cause Q to equal $1/\sqrt{2}$ will be;

$$R = (\sqrt{2}) \cdot \frac{\sqrt{180\ nH}}{\sqrt{65pF}} \text{ ohms}$$

which yields; R = 74.4 ohms

Since the equivalent series output resistance of the device is 44 Ω (as shown in Figure 2), an additional 30.4 Ω must be added in series with the output in order to make the total resistance equal to 74.4 Ω. Figure 4 shows the frequency response of the above set-up along with the uncompensated response. For this graph, a 33 Ω resistor was used and a 60 pF load capacitor simulated the additional disabled devices.

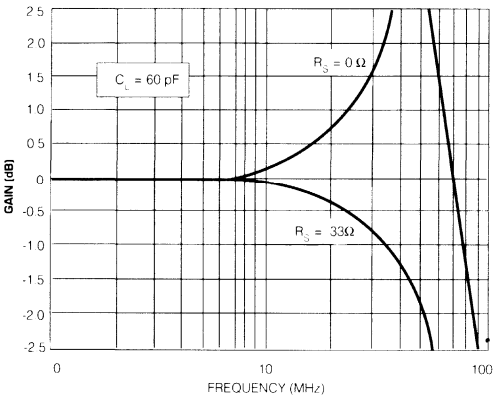


Fig. 4 Frequency and Uncompensated Responses

With the same 33 Ω resistor in the circuit, the load capacitors were changed to 47 pF and 27 pF in order to see their effects on the frequency response. The 47pF capacitor closely simulates a 16 x 1 crosspoint circuit while the 27 pF approximates a 10 x 1 situation. Figure 5 shows the results of these changes.

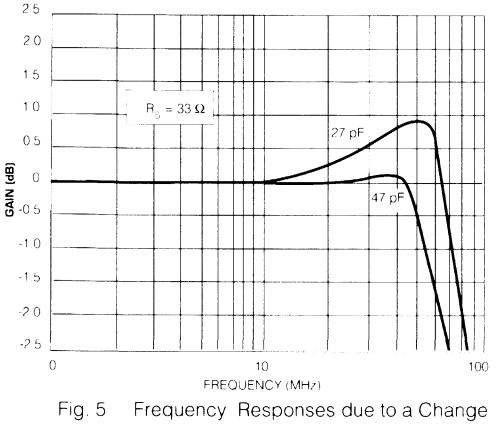


Fig. 5 Frequency Responses due to a Change of Capacitor Values

Precise modelling has been done yielding far more accurate results. The effect on the frequency response of any series compensating resistor can be computer simulated using these models. Figure 6 is an engineer-generated model of the GX414 or GX424 device. This model has been simulated using 'PSpice' (software by MicroSim Corporation) and compared to measured results. A PSpice NETLIST is available on floppy disk from Gennum for assisting the systems engineer and designer. The input and output impedance parameters are specified for frequencies up to 70 or 80 MHz and will produce accurate frequency response results for load capacitances between 10 pF and 100 pF.

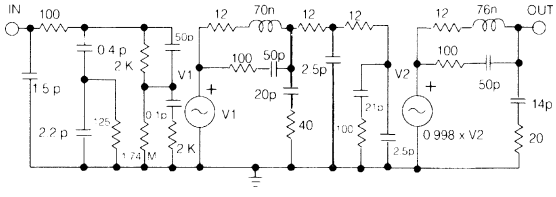


Fig. 6 Engineer-generated Model of GX414 or GX424

Figure 7 is an approximate model of a disabled crosspoint switch showing some of the circuit potentials and more importantly, the various capacitances associated with a disabled switch.

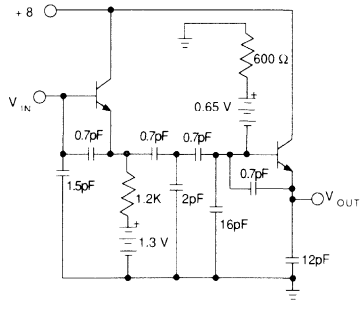


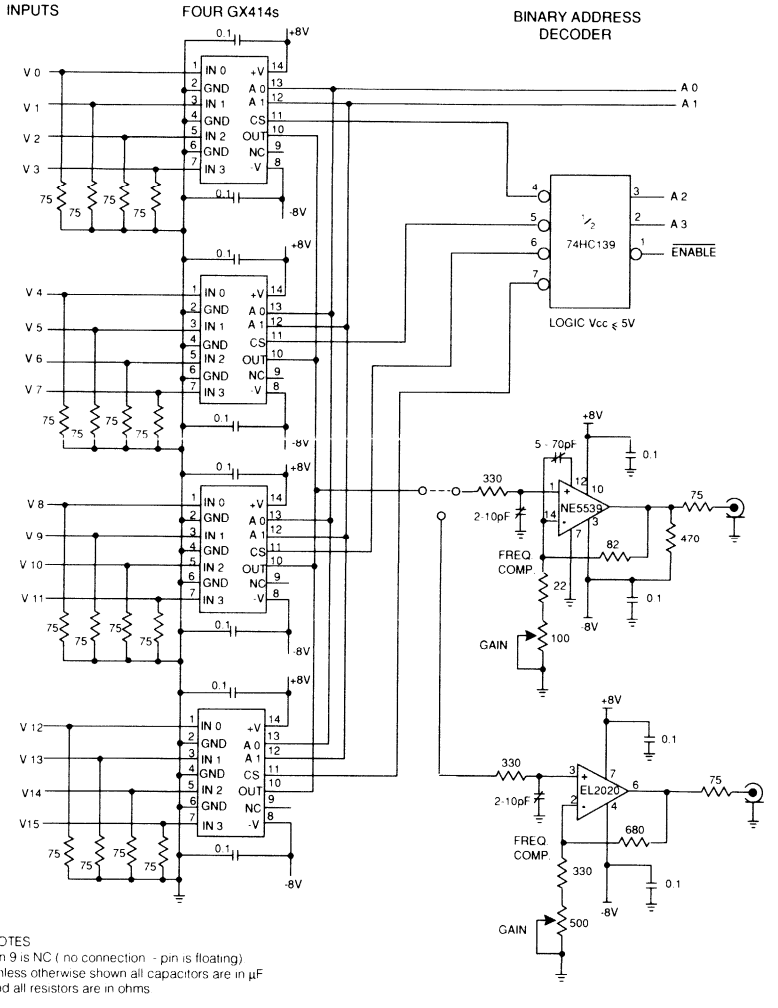
Fig. 7 Disabled Crosspoint Equivalent Circuit

The input capacitance of a disabled switch varies with the DC bias voltage from 2.1 pF at -1 volt to 2.5 pF at +1.5 volts. Futhermore, there is a slight change in C_{IN} between the disabled state (2.2 pF at 0 volts bias) and enabled state (2.0 pF at 0 volts bias). The slight variations would only be significant if the input driver source impedance is high. The output capacitance of the disabled chip is made up of four times 0.7 pF, for the four output transistors, plus 12 pF which is common to all outputs, giving a total of approximately 15 pF.

Method 2. Frequency Compensation by the Output Buffer Stage.

The only drawback of using a series resistor to compensate for the peaking response of the GX414 and GX424 is the slight degredation of differential phase through the switch and resis tor. Since the outputs are eventually buffered at the bus by an operational amplifier or a specifically designed video buffer, it seems reasonable to compensate at this point in the system.

Figure 8 shows a 16 x 1 system that is set up using four GX414's and two popular buffer amplifiers. The first is an Elantec EL-2020 and the second is a Signetics NE-5539. The EL-2020 is a 50 MHz current feedback amplifier specifically designed for use in video applications. The NE-5539 is an ultra-wideband operational amplifier having an external frequency compensation pin.



NOTES
Pin 9 is NC (no connection - pin is floating)
Unless otherwise shown all capacitors are in μF and all resistors are in ohms

Fig. 8 16 x 1 Video Crosspoint Circuit

Several combinations of resistor values were used in order to set the gain of each amplifier to 6 dB and yet maintain stability. A small trimmer capacitor in conjunction with a series resistor was used as a lag-circuit at the amplifier input. Along with this circuit, in the case of the NE-5539, a compensating trimmer capacitor was connected to the compensation pin.

Each buffer amplifier was then independently connected to the 16 x 1 crosspoint circuit and the variable circuit elements were adjusted to flatten the frequency response. The frequency response was observed and measured using the test set-up as shown in Figure 9.

Initially, the buffer amplifiers were set up having as wide a bandwidth as possible. Results approaching those shown in the manufacturer's data book were achieved. The crosspoint switches were then placed in the circuit and obvious amounts of frequency peaking were noticed.

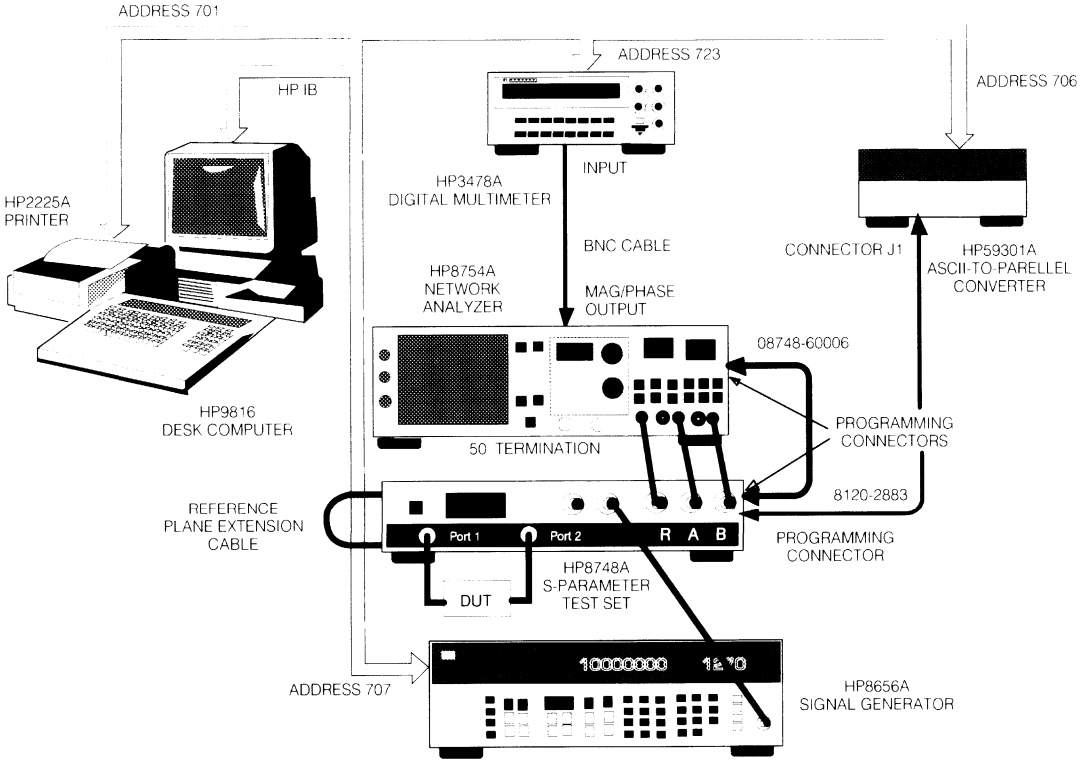


Fig. 9 Test Set-up

The lag-circuit trimmer, the compensating trimmer and gain potentiometers were adjusted until a flat response was achieved. Figures 10, 11 and 12 show the various frequency response results.

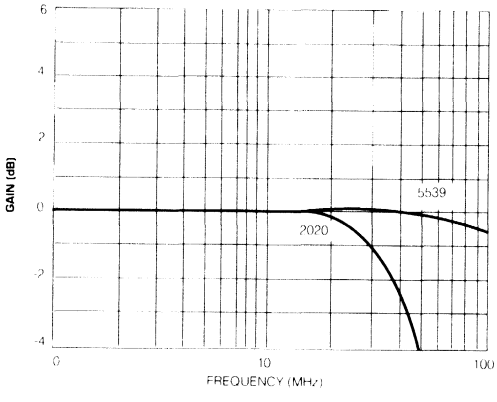


Fig. 10 Amplifier Response

The wide bandwidth of the NE5539 is obvious with a -3dB frequency of well over 200 MHz, while the -3dB point of the EL-2020 is about 45 MHz.

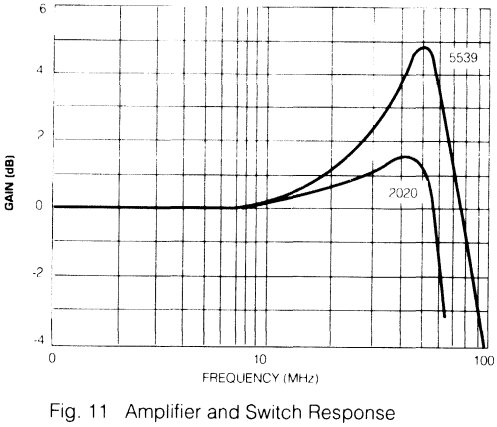


Fig. 11 Amplifier and Switch Response

Predictable peaking occurs in both systems between 40 and 50 MHz.

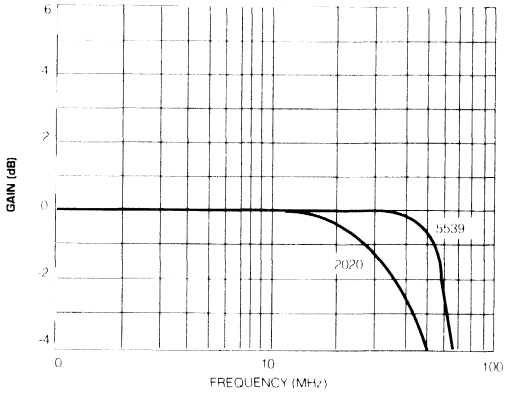


Fig. 12 Resultant Flat Response

Virtually all peaking has been removed, resulting in a flat response to at least 35 MHz for the NE5539 and at least 15 MHz for the EL-2020.

CONCLUSION

This brief application note has dealt with the compensation for flatness that is necessary when using the GX414 and GX424 video crosspoint switches. The video system designer is concerned with flatness and insertion loss of any crosspoint switch in his system at the colour burst frequencies of either 3.58 MHz or 4.43 MHz.

The insertion loss of the GX4 family of devices at these frequencies is less than 0.05 dB. However, for wideband and high bit rate data, it is important to have a flat response, out to at least 30 to 50 MHz. Using the techniques described in this application note in conjunction with the buffer stages specified, the GX414 and GX424 switches can be made to have a flat response up to the frequencies mentioned above.

Indeed, the peaking response of the GX414 and GX424 can be used to advantage with a falling response found in most operational amplifier circuits in order to flatten the overall frequency response.

Application engineers at Gennum are more than happy to work along with system designers and will try to answer any customer questions regarding the GX414 and GX424, high performance Video Crosspoint Switches.

16x1 VIDEO CROSSPOINT EVALUATION BOARD

by Ian Ridpath, Senior Application Engineer, Video and Broadcast Products Group

APPLICATION NOTE

INTRODUCTION

This application note describes the construction and use of the GENNUM 16x1 Video Crosspoint Evaluation Board. This board is intended to demonstrate the straight forward application of the GX414, GX414A, GX424 and GX434 video crosspoint switches in a 16x1 multiplexer configuration.

DESIGN FEATURES

In addition to the crosspoint switches, this board incorporates address decoding and disable logic and an output buffer amplifier. With a total parts count of only 28 (excluding optional DIP sockets and I/O connectors), the Gennum 16 x 1 circuit represents the simplest, most cost effective and lowest power consumption 16 x 1 video crosspoint module available. (See note 1, page 5)
Other features are highlighted below.

* Extremely low differential gain and phase (final result depends on buffer amplifier used).

* Extremely high OFF isolation and low crosstalk.

* Virtually no switching *glitches*.

* No external buffer transistors are needed in order to keep the ON to OFF input impedance constant.

* Less than 30 mW disabled power consumption

The on board video buffer allows the multiplexed video signal to directly feed a 75Ω load. An additional unbuffered video output allows the user to parallel up several boards and connect an external buffer.

THEORY OF OPERATION (refer to Figure 1)

Each crosspoint IC has a $\overline{\text{Chip Select}}$ and two Address inputs which operate according to the following truth table.

TRUTH TABLE

$\overline{CS}$	A1	A0	OUTPUT
0	0	0	IN 0
0	0	1	IN 1
0	1	0	IN 2
0	1	1	IN 3
1	X	X	HI - Z

X = DON'T CARE

If more than one device is used, the ADDRESS inputs for each device are simply connected in parallel. The address selection bits are A0 and A1 and determine which of the four crosspoints per device are activated. However, until the chip has been selected (chip select = 0), no signal path exists.

The four $\overline{\text{Chip Select}}$ inputs must be decoded from the two most significant address bits, A2 and A3. Furthermore, all the devices must be turned off if none of the 16 video inputs (IN1 to IN16) are required (circuit disabled). This decoding and disabling is accomplished by one half of an MM74HC139N dual 2 to 4 decoder.

The two most significant address bits are applied to pins 2 and 3 of this device. When the device is enabled (low on pin 1), a unique low state output is generated at the output (pins 4, 5, 6 or 7). When the 74HC139 IC is disabled, (Disable = 1), all the outputs go high and turn off all four GX4 devices. In this manner any one of sixteen video paths can be selected or all can be turned off by using five bits of data (A0,A1,A2,A3 and Disable.)

The video input signals are directly connected to the video switches. If these signals are fed from a 75 Ω cable, a 75 Ω resistor should be installed from the input to ground. In multi-input applications where the input is driven from a low impedance buffer amplifier, these 75Ω resistors are not needed. All unused inputs should either be tied directly to ground or tied down with 75 Ω resistors.

Assuming that a video signal on input 1 (IN 1) is required to be switched to the output, the data bits should be as follows;

A0 = 0,
A1 = 0,
A2 = 0,
A3 = 0,
DISABLE = 0 (enabled).

In this case, the first of the four crosspoint switches in IC1 is selected by address bits A0 and A1. Pin 4 of IC5 goes low because address bits A2 and A3 are low and because pin 1 of the device is low (low = enable).

The low logic level coming from pin 4 of IC5, creates a chip selection for IC1, enabling the crosspoint and allowing the video signal on IN-1 to be routed to pin 10. From here it goes to the buffer amplifier, IC6 via the 22 Ω series resistor, R1 and a lag circuit made up of R5 and C12.

Document No. 510 - 48

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The series resistors R1-R4 dampen the Q of the frequency peaking response of the crosspoint switches and the lag circuit further tailors the frequency response in order to produce a flat response (see note 2, page 5). The gain of the buffer is nominally set for 2 (+6 dB) by the trimpot, R9, in order to compensate for the loss through the 75 Ω back matching resistor, R8. Similarly, if the video signal on IN16 was selected, the data bits would have to have the following logic levels:

A0 = 1, A1 = 1, A2 = 1, A3 = 1, DISABLE = 0.

In this case, the fourth switch in IC4 would be activated and that chip would be selected by the low output on pin 7 of IC5.

Unbuffered video can be observed at the Unbuffered Video Output. When this output is used, a load resistance of 10 kΩ or greater should be used. The frequency response will be relatively flat up to 40 MHz or 50 MHz and is not dependent upon the response of the on board buffer.

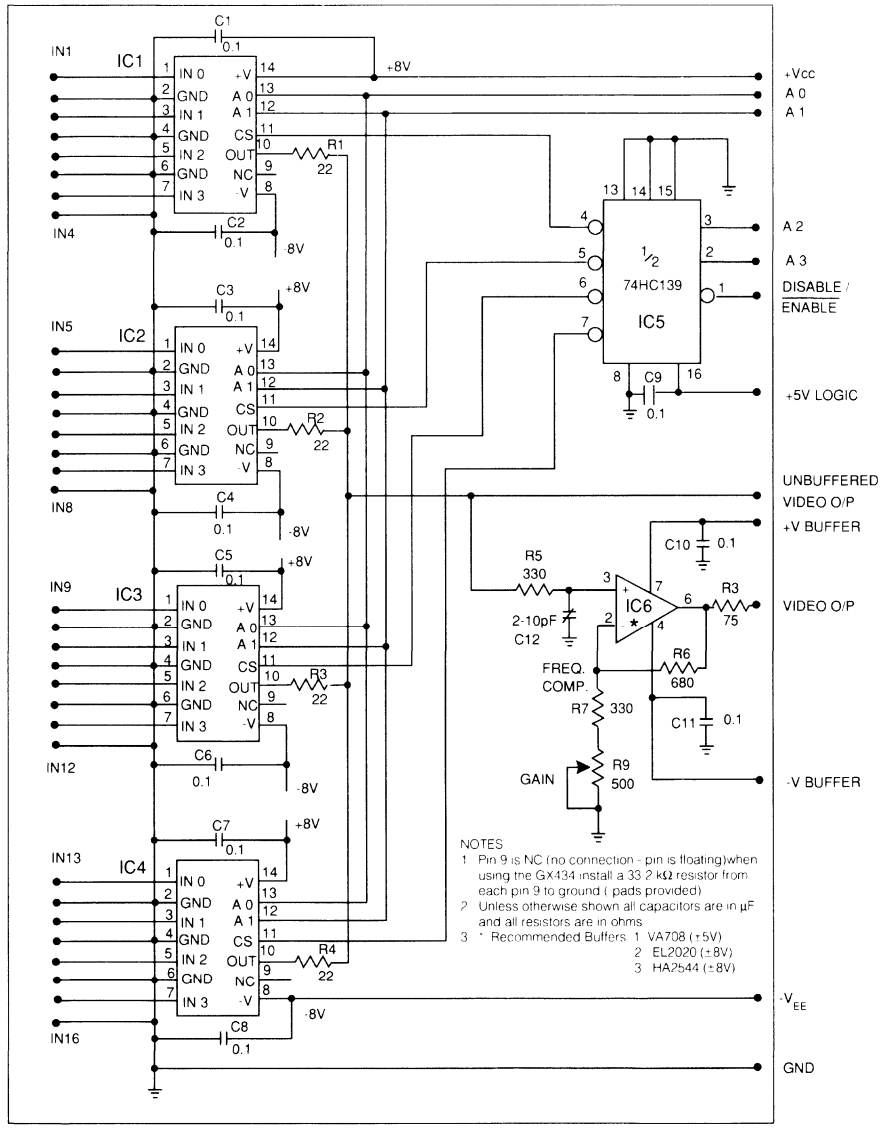


Figure 1 Circuit Diagram of the 16 x 1 Video Multiplexer Board

The power supply connections for the video buffer amplifier are independent of the rest of the circuit. The board is laid out to accept any of several video buffer amplifiers having the standard opamp pin-outs as shown. Many of these can operate from the same V_{CC} and V_{EE} as does the rest of the board. One amplifier recommended however, is the VA708 video buffer from VTC which has a maximum supply voltage rating of only 6 volts.

The power supply voltage for the logic must not exceed 5.25 volts. This allows the use of either LS-TTL or 5 volt HCMOS. There is however, an increase of 35 mW power consumption when LS-TTL is used.

CONSTRUCTION AND SET-UP

Artwork for the PCB is included in this application note along with a parts list and typical performance results. Construction is straight forward and should present no real problems. An etched and drilled PCB is available from Gennum Corporation at a nominal price. Those interested in obtaining a board should contact the Video/Broadcast Products Group at Gennum.

Two possible test set-ups are described in this application note. They are shown in Figures 2 and 3. One uses the on-board buffer amplifier and the other is for use with an external buffer. In either case, the address and enable logic levels can be generated by DIP switches or the outputs of shift registers and/or latches. If DIP switches are used, pull-up resistors must be included.

Also, if the buffer amplifier is capable of operating at the same supply voltages as the crosspoints, the appropriate supply pins can be wired together. This would leave only the logic

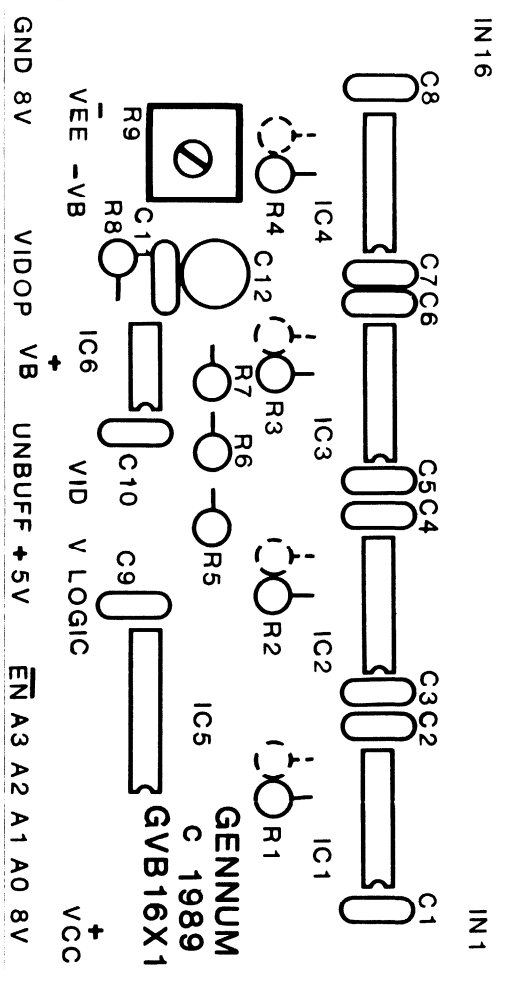


Fig. 4 Component Layout on PCB (actual size)

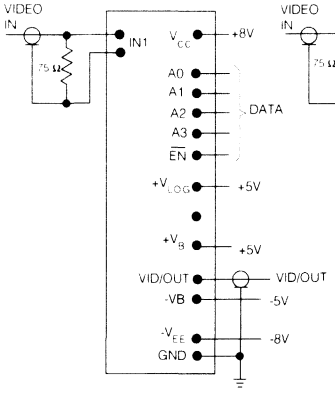


Fig.2 Test Circuit 1
(On-board Buffer)

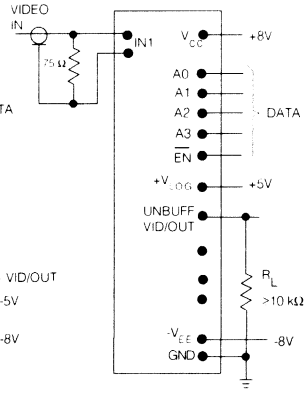


Fig. 3 Test Circuit 2
(External Buffer)

NOTE: -VB may be connected to $-V_{EE}$
+VB may be connected to $+V_{CC}$

Parts List

Qty	Description	Designation
1	Printed Circuit Board Gennum Corp (GVB16X1)	
4	GX414CD IC Gennum Corp	C1 to IC4
1	MM74HC139N IC National	IC5
1	VA708 or EL2020 or HA2544 video buffer IC	IC6
11	0.1 µF,100 V block capacitor	C1 to C11
1	2 to 10 pF trimmer capacitor	C12
4	22Ω, 1/4W, 1% resistors	R1 to R4
2	330Ω, 1/4W, 1% resistors	R5, R7
1	680Ω, 1/4W, 1% resistor	R6
1	75Ω, 1/4W, 1% resistor	R8
1	500ΩPCB mount trimpot	R9
4	14 pin DIP sockets (optional)	
1	16 pin DIP socket (optional)	
1	8 pin DIP socket (optional)	
4	8 way strip connectors (0.1 in.) (optional)	
13	PCB connector terminals (optional)	

Test Results

Using test circuit 1 with a VA708 buffer amplifier, the following quantities were measured and calculated:

Crosspoint supply voltage	=	± 8 V
Buffer amplifier supply voltage	=	±5 V
Logic supply voltage	=	+5 V
1. Positive crosspoint supply current (disabled)	=	1.65 mA
2. Negative crosspoint supply current (disabled)	=	1.00 mA
3. Positive crosspoint supply current (enabled)	=	11.42 mA
4. Negative crosspoint supply current (enabled)	=	10.74 mA
5. Logic supply current (74LS139)	=	7.00 mA
6. Logic supply current (MM74HC139)	=	0.10 mA
7. Buffer Amplifier positive supply curent	=	8.40 mA
8. Buffer amplifier negative supply current	=	8.40 mA
9. Total DISABLE power consumption (74LS139)	=	140 mW
10. Total ENABLED power consumption(75LS139)	=	296 mW
11. Total DISABLED power consumption (74HC139)	=	105 mW
12. Total ENABLED power consumption (74HC139)	=	262 mW
13. Frequency response - 0.1 dB	=	20 MHz
- 1.0 dB	=	32 MHz
- 3.0 dB	=	42 MHz

Using test circuit 2 with no on board buffer amplifier, the following quantities were measured and calculated.

Crosspoint supply voltage	=	± 8 V
Logic supply voltage	=	+ 5 V
1. Positive crosspoint supply current (disabled)	=	1.65 mA
2. Negative crosspoint supply current (disabled)	=	1.00 mA
3. Positive crosspoint supply current (enabled)	=	11.42 mA
4. Negative crosspoint supply current (enabled)	=	10.74 mA
5. Logic supply current (74LS139)	=	7.00 mA
6. Logic supply current (74HC139)	=	0.10 mA
7. Total DISABLED power consumption (74LS139)	=	56.2 mW
8. Total ENABLED power consumption (74LS139)	=	212 mW
9. Total DISABLED power consumption (74HC139)	=	21.25 mW
10. Total ENABLED power consumption (74HC139)	=	178 mW
11. Frequency response (crosspoints alone)		
IN 16 +2.0 dB	=	42 MHz
-1.0 dB	=	65 MHz
-3.0 dB	=	80 MHz

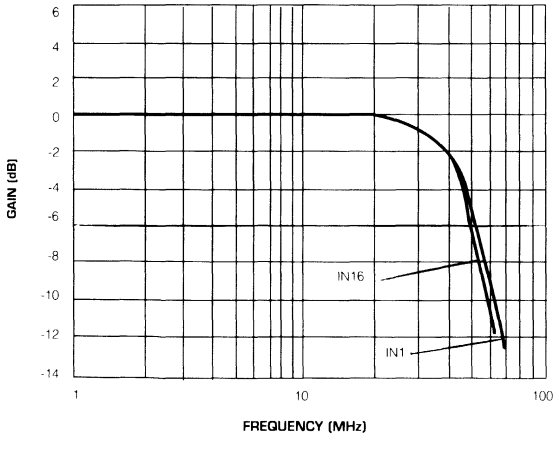


Fig.5 Frequency Response of Test Set-up 1

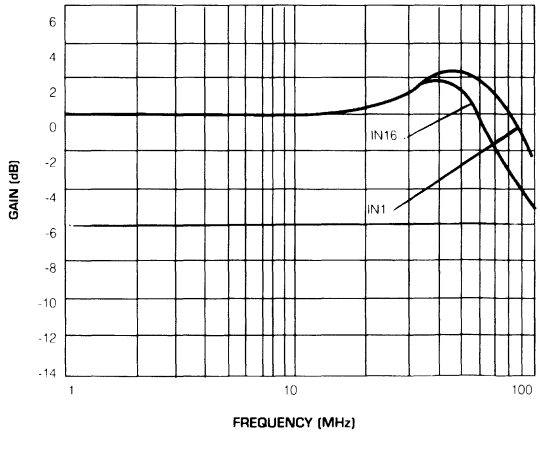
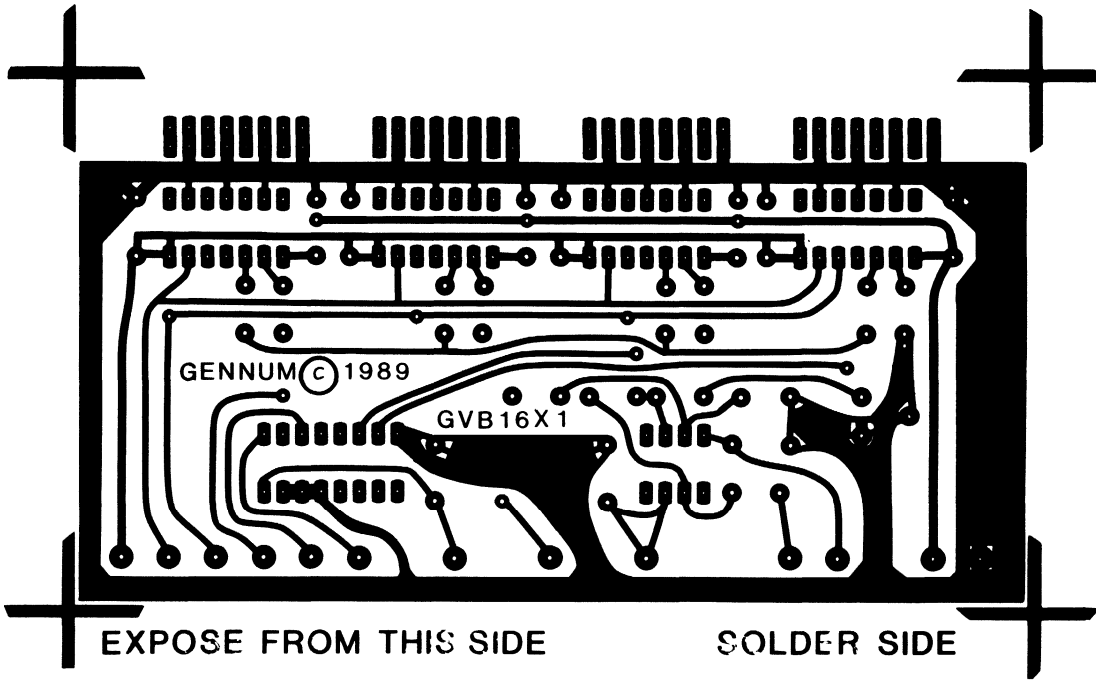
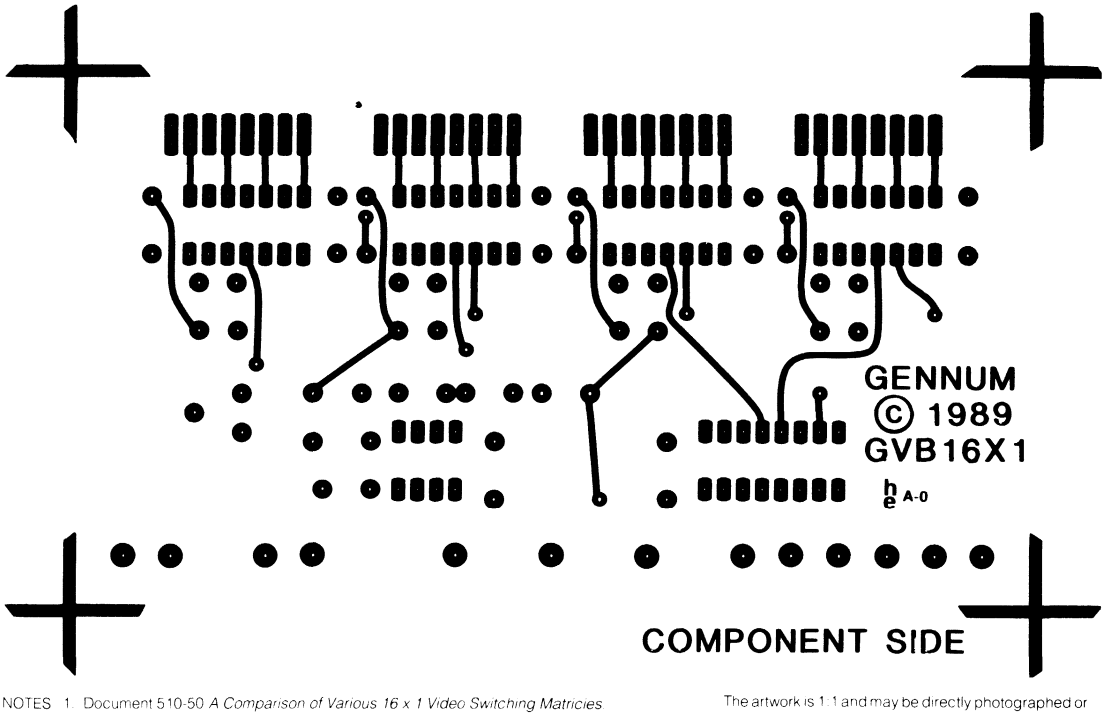


Fig.6 Frequency Response of Set-up 2

Printed Circuit Board Artwork





NOTES 1. Document 510-50 *A Comparison of Various 16 x 1 Video Switching Matricies*.
2. Document 510-39 Application Note *Frequency Peaking Compensation of the GX414 and GX424* (available from Gennum Corporation).

The artwork is 1:1 and may be directly photographed or copied. If plated through-hole facilities are not available, the pad-vias may be made by using tinned copper wire.

Parameter Netlist for GX414 and GX424 FILE: MODL414.CIR

INPUT				MID-CIRCUIT				OUTPUT			
C1	1	0	1.5P	C3	4	5	8P	R10	8	11	65
R1	1	2	65	R6	4	7	11.8	R11	11	12	1500
R2	2	3	1500	R3	5	0	100	C11	11	14	0.3P
C2	2	4	60P	C6	7	0	2.5P	C10	11	16	60P
C4	2	6	0.3P	R7	7	8	11.8	V2	12	16	DC 0
V1	3	4	DC 0	C7	8	0	10P	C13	14	0	2.2P
C5	6	0	2.2P	R8	8	9	10K	R13	14	0	25
R5	6	0	25	R9	8	10	80	F2	14	16	V2 125
F1	6	4	V1 125	C8	9	0	10	R12	14	16	33K
R4	6	4	33K	C9	10	0	15P	R14	15	0	20
								C12	15	16	14P

Figure 3 shows how the signal source and load capacitance are connected to the model.

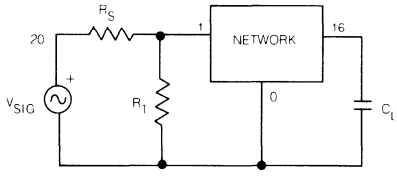


Figure 3

The load capacitance between nodes (16) and (0) is specified as :

CL 16 0 ---P (NOTE 10 pF < CL < 100 pF)

and the input ac source between nodes (1) and (0) is specified as:

V_{SIG}	20	0	AC	<amplitude> <phase>
R_S	20	1	75	
R_T	1	0	75	

(if $R_S = R_T$, then <amplitude> = 2, <phase> =0)

Note that node (20) is the junction of the generator and its internal source resistance R_S.

The following PSpice® commands are used in this file.

- OPTIONS LIMPTS = 20000,NOMOD,NOPAGE
- AC DEC 50 1MEG 100 MEG
- PRINT AC VDB (16) VP (16)
- PROBE
- END

These allow for the printing in tabular form of the output voltage in dB and phase in degrees versus frequency from 1 to 100 MHz. The •PROBE statement will allow for the graphical representation of the output data using PSpice® PROBE.

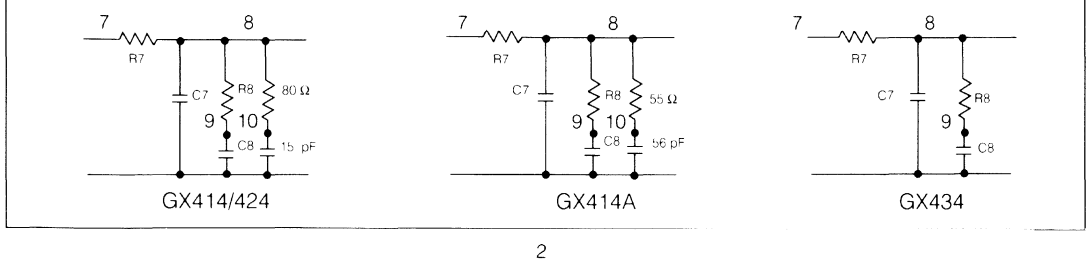
GX414A & GX434

The variations for the GX414A and GX434 devices are highlighted below. It should be noted that only one portion of the crosspoint circuit is altered.

For the GX414A, the value of R9 is changed from 80 Ω to 55 Ω and the value of C9 is changed from 15 pF to 56 pF. For the GX434 device, both of these frequency compensation components are removed.

Figure 4. shows in detail, this area of the crosspoint equivalent circuit.

Figure 4



Parameter netlist for the GX414A FILE: MODL414A.CIR

As per MODL414.CIR with the following changes.

R9	8	10	55
C9.	10	0	56P

Parameter netlist for the GX434 FILE: MODL434.CIR

As per MODL414.CIR without R9 and C9.

The output data generates typical performance curves which compare favorably with measured results. The spread in results can be predicted by looking at the GAIN SPREAD curves on the associated device DATA SHEETS.

This PSpice® design 'tool' can be used to determine the value of the series compensating resistor required to flatten the overall frequency response of a multiplexer system.
(See Application Note No.510-39, FREQUENCY PEAKING COMPENSATION OF THE GX414 AND GX424, available from Gennum Corporation).

The application engineers in the Video and Broadcast Products Group at Gennum Corporation will assist in answering any questions or providing any additional engineering information.

Floppy disks with the netlist files are available from the above source.

HDTV 8x1 and 10x1 Modular Multiplexers

APPLICATION NOTE

by Ian Ridpath, Senior Applications Engineer, Video and Broadcast Group

INTRODUCTION

High definition TV places additional requirements on crosspoint performance in video switching systems. These include a wider flat frequency response and better high frequency off-isolation and crosstalk performance. In larger routing matrices, such considerations as ease of I/O connections, expandability and repeatability of system parameters from channel to channel, become even more important.

The modular multiplexers described in this application note, take these, as well as other points, into consideration and provide an optimal solution for the video design engineer. The multiplexers are realised using Gennum's GX4201 wideband 1x1 crosspoint IC.

FUNCTIONAL DESCRIPTION

Figures 1 and 2 are functional block diagrams of the 8x1 and 10x1 modules. In both cases, the 1x1 crosspoint ICs are multiplexed to form the desired circuit configuration.

On the 8x1 version, a single CMOS device performs 3 to 8 line decoding as well as latching using a STROBE input. The ENABLE input allows the entire module to be selected or disabled in order to facilitate the multiplexing of other modules.

The 10x1 module uses a single BCD-to-decimal decoder for crosspoint selection. By applying a binary code greater than 1 0 0 1 (9), all crosspoint devices can be turned off. This as in the 8x1 module, effectively turns off all crosspoints. Both modules use ±5 V supplies for the crosspoints. The logic ICs require +5 V only.

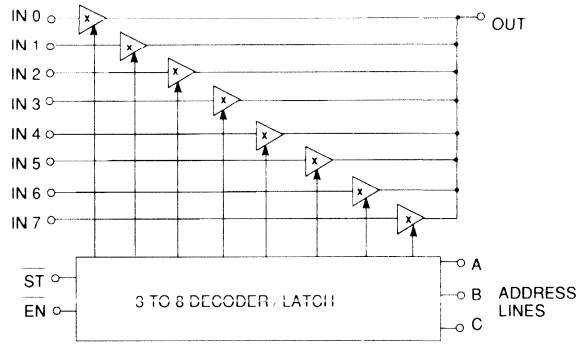


Figure 1

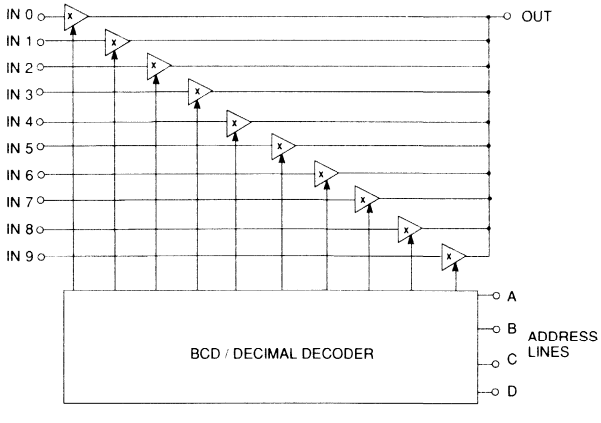


Figure 2

CIRCUIT DESCRIPTION

CROSSPOINT DEVICES (see Figures 3 and 4)

Each GX4201 device is a 1x1 video crosspoint characterised by a low distortion, unilateral signal path consisting of emitter followers at the input and output with level shifting circuits in between.

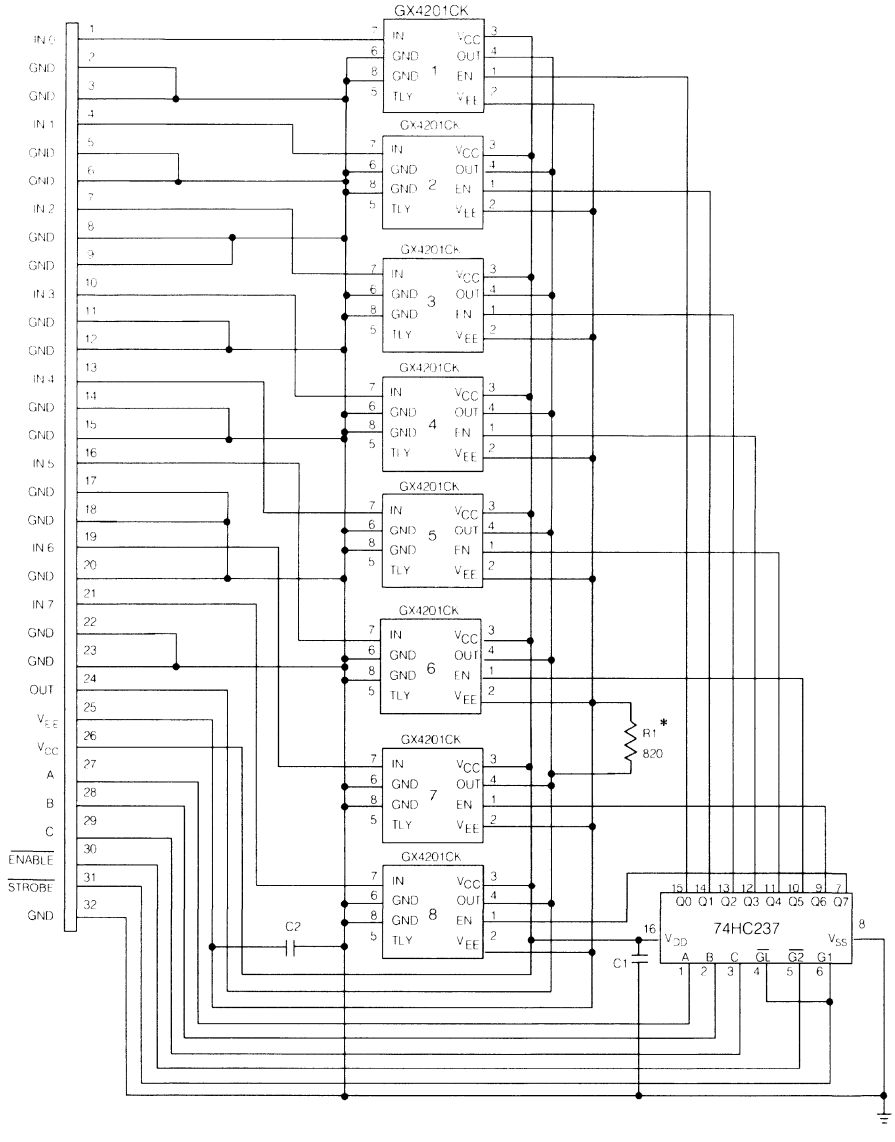
Extemely high off-isolation in the order of 80 dB at 100 MHz is achieved by internal clamping in the signal path. The input impedance is extremely high and constant, allowing for multi-input bussing.

The input may be directly driven from cables if a terminating resistor, equal to the characteristic impedance of the cable, is connected from input to ground.

The output requires a high impedance load of at least 10 kΩ to maintain the high degree of differential gain and phase, characteristic of the crosspoint devices.

The device data sheet is available from Gennum corporation by ordering document number 510-74. It fully describes the operation of the device along with electrical characteristics and performance curves.

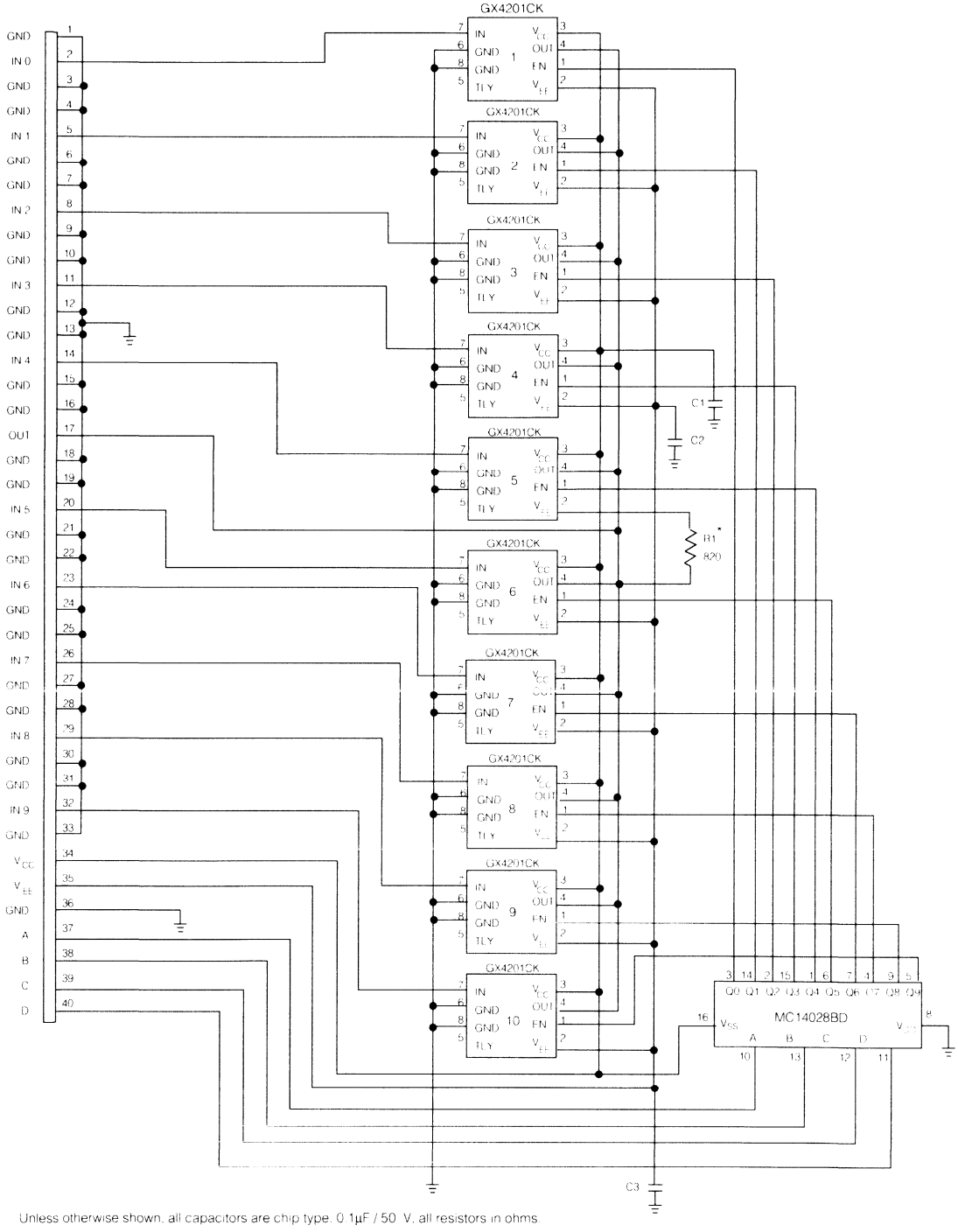
Document No. 510 - 84



Unless otherwise shown, all capacitors are chip type, 0.1µF / 50 V, all resistors in ohms.

* This resistor may be external or an external 6mA current source may be used.

Fig. 3 8x1 Multiplexer Module



Unless otherwise shown, all capacitors are chip type, 0.1μF / 50 V, all resistors in ohms.

* This resistor may be external or an external 6mA current source may be used.

Fig. 4 10x1 Multiplexer Module

LOGIC DEVICES

The 8x1 module uses a CMOS 74HC237 combination 3 to 8 decoder/latch for crosspoint selection, the 10x1 module uses a Motorola MC14028B BCD-to-decimal decoder.

Figure 3 shows the eight GX4201 devices with their outputs tied together effectively forming an 8x1 multiplexer. Pin 1 of each device is an ENABLE input requiring a logic HIGH level in order to turn on the crosspoint. The logic level is provided by the 74HC237 device.

Address A, B and C control the decoder so that only one output goes HIGH for any of the eight address possibilities.

An ENABLE input on the 74HC237 is used to disable the decoder inputs resulting in all the outputs going to a logic LOW state. This causes all the GX4201 outputs to go to their high impedance state, effectively disabling the module, simplifying the multiplexing of additional modules.

All address bits are internally latched by the 74HC237. The STROBE input is used as the clock for the latches and operates on the transition from logic LOW to HIGH.

An 820 Ω resistor is connected from the negative power supply rail to the output. This is a current source for the GX4201 devices.

Video is applied to pin 7 of each crosspoint. The adjacent pins are connected to ground in order to maintain a high degree of channel to channel isolation. The output of each device (pin 4) is connected to the corresponding output of the other seven switches.

Both positive and negative supply voltages are routed to each device. Capacitors C1, C2 and C3 function as supply rail decoupling capacitors.

The 10x1 circuit, Figure 4, is very similar to the 8x1circuit. In this case, two additional GX4201 crosspoint devices have been added and the decoding function is performed by the MC14028B. Address bits A,B,C and D are used for crosspoint selection. As in the 8x1 circuit, the functions of the 820 Ω resistor and the 3 capacitors are identical.

PIN CONNECTIONS

In designing these video multiplexers, careful consideration was given to assignment of pin connections. Figures 5 and 6 show the resulting pin outs.

Ground pins separate each video input, and the video inputs are situated to one end and in the middle of each module. It is therefore, straightforward to parallel additional module inputs.

The video output pin on the 10x1 module is separated from any input by two ground pins. Furthermore, the output is brought out midway between the inputs to maintain somewhat equal signal path lengths.

All power supply and logic functions are brought out at one end of each module. This allows for simplified multiplexing of additional modules.

MODULE OPERATION

The Truth Tables shown in Figures 7 and 8 describe the operation of the modules.

C	B	A	EN	ST	OUT
X	X	X	1	X	HI-Z
X	X	X	X	0	HI-Z
0	0	0	0	↓	IN 0
0	0	1	0	↓	IN 1
0	1	0	0	↓	IN 2
0	1	1	0	↓	IN 3
1	0	0	0	↓	IN 4
1	0	1	0	↓	IN 5
1	1	0	0	↓	IN 6
1	1	1	0	↓	IN 7

X : DON'T CARE

Figure 7

D	C	B	A	OUT
0	0	0	0	IN 0
0	0	0	1	IN 1
0	0	1	0	IN 2
0	0	1	1	IN 3
0	1	0	0	IN 4
0	1	0	1	IN 5
0	1	1	0	IN 6
0	1	1	1	IN 7
1	0	0	0	IN 8
1	0	0	1	IN 9
1	0	1	0	HI-Z
1	0	1	1	HI-Z
1	1	0	0	HI-Z
1	1	0	1	HI-Z
1	1	1	0	HI-Z

Figure 8

Figure 5

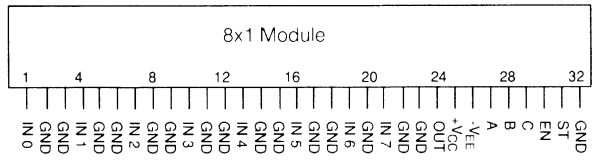
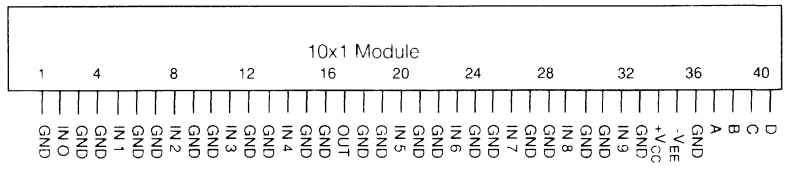


Figure 6



For the 8x1 version, the module is enabled with a logic LOW on the $\overline{\text{ENABLE}}$ input, the output reflects the latched input selected by ADDRESS BITS A, B and C when the $\overline{\text{STROBE}}$ input is returned from a logic LOW to a logic HIGH.

In the 10x1 version, there is no laching and the module is disabled by applying a binary code greater than 9 to the address inputs A, B, C and D.

Since each video input is represented by a high impedance, several inputs may be bussed to form multi-input matrices. It is important in these situations to follow careful motherboard layout, as well as use ample groundplane.

The bussed inputs should be driven from a stable, low impedance buffer amplifier. In some case, a small value series resistor at each video input will prevent unwanted R.F. oscillations.

PRINTED CIRCUIT BOARDS

The printed circuit boards are 0.03125 inch glass epoxy, double-sided material with one ounce copper.

All componants are surface mounted except for the input/output pins, which are 'finger' type leadframes and are soldered to both the componant and 'copper' side of the board.

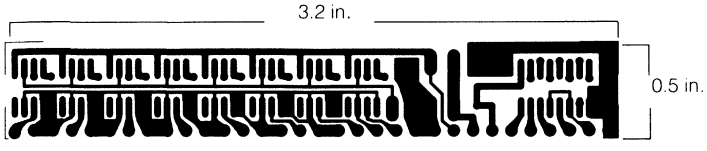


Fig. 9 Component Side 8x1

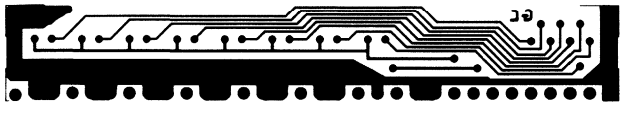


Fig. 10 Copper Side 8x1

NOTE;
All layouts are shown in actual size.

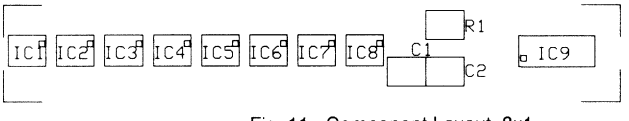


Fig. 11 Component Layout 8x1

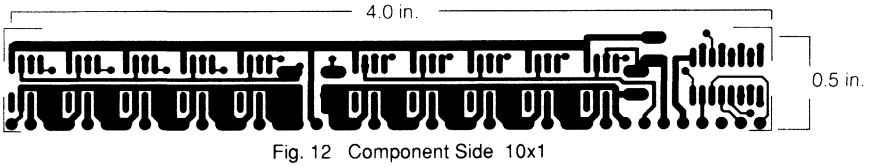


Fig. 12 Component Side 10x1

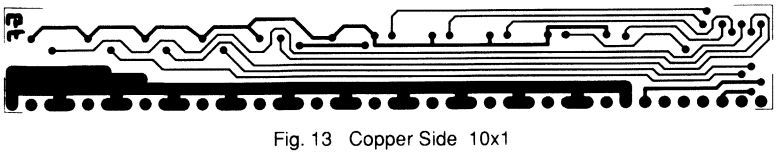


Fig. 13 Copper Side 10x1

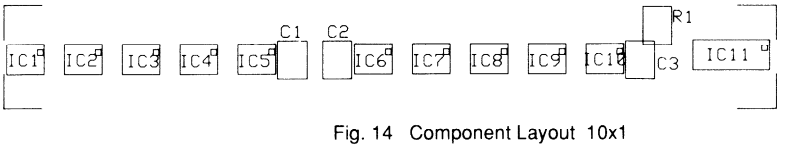


Fig. 14 Component Layout 10x1

TESTING PERFORMANCE

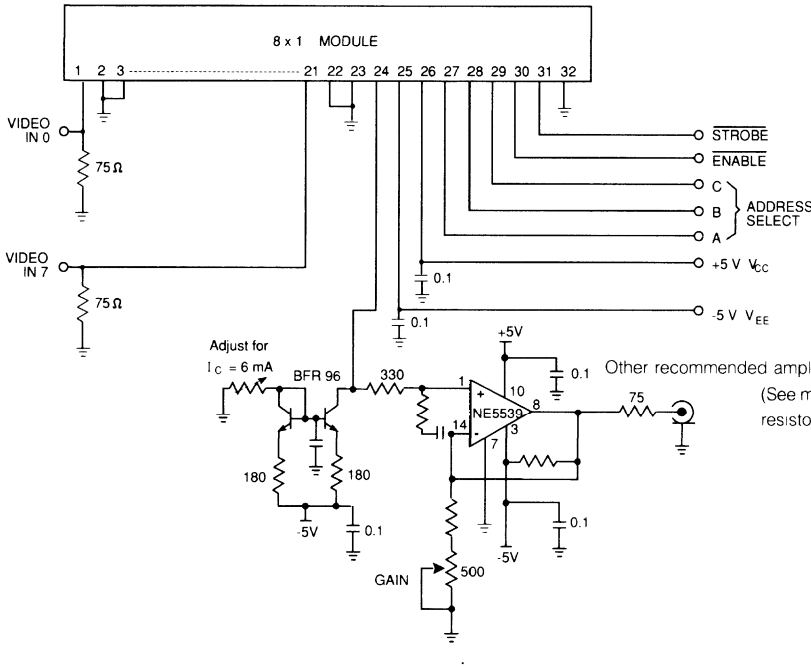
Once the assembly of the modules is complete, the task of testing and evaluating the performance can be achieved using a suitable test jig.

The jig itself should be constructed using careful R.F. design techniques for the video signal paths. Suitable power supply decoupling capacitors should be used for each of the three supplies. Address selection can be made using toggle, DIP or decoded thumbwheel switches. Each one of the logic inputs requires a 10 kΩ pull-up resistor.

The two test jigs used are shown in Figures 15 and 16.

Critical measuements of differential gain and phase can be taken using a wideband network analyser such as the Hewlett-Packard 4195A. A video vectorscope can also be used but will result in a less accurate measurement.

As far as the frequency response is concerned, the network analyser can be used to produce extremely accurate results. The advantage of using a network analyser, such as the 4195A, is that a hardcopy plot may be obtained for any measurement made. Also, the measurement set-up data can be stored for repeated tests.



Other recommended amplifiers are CLC410,EL2030 (See manufacturer's data sheets for resistor values).

Fig. 15 Test Jig 8x1

NOTES:

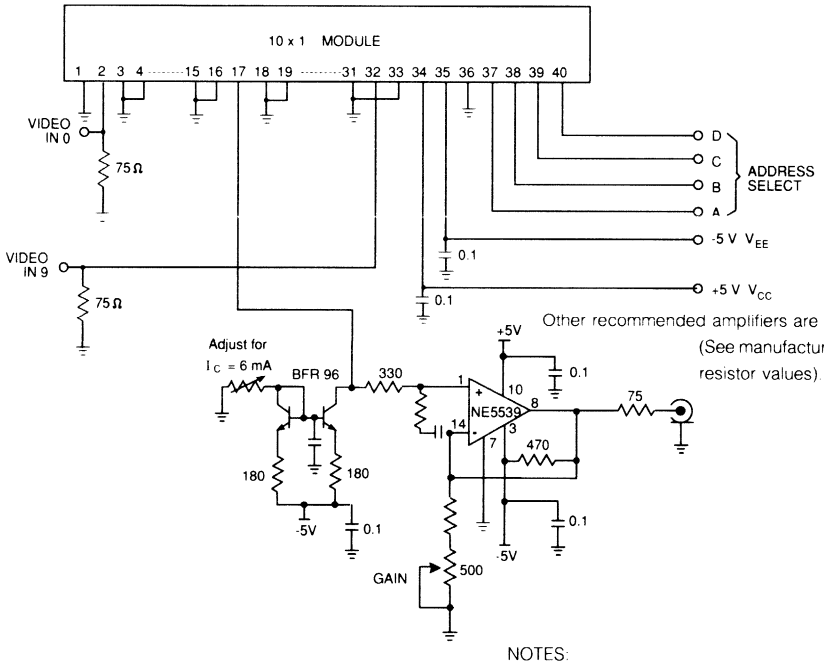
1. All logic inputs require a 10 kΩ pull-up resistor.
2. The BFR 96 current source circuit may be replaced with an 820 Ω resistor to V_{EE}. This will result in a slight increase in insertion loss.
3. All capacitors are chip type. 0.1 μF/50 V.

The buffer amplifier shown is an NE5539 ultra wideband operational amplifier. Other amplifiers such as the Elantec EL2030 and the Comlinear CLC110 unity gain buffer and the CL410 video output buffer gave similar results. (It should be remembered that the signal path without the modules is initially normalised before any measurements are taken with the network analyser).

Where this is not the case, the amplifier should be adjusted to have a flat frequency response, to at least 100 MHz.

In order to measure off-isolation and all-hostile crosstalk, of the modules themselves, the inputs must be extremely well shielded and careful attention must be paid to the lead dress. When using the network analyser, the measurements involve applying a +15 dBm signal to the OFF switch in order to maintain the noise floor below 100 dB. This level must be reduced to -20 dBm for tests on ON switches.

Figure 17a through 17f show typical results obtained using the test jigs described here.



Other recommended amplifiers are CLC410,EL2030 (See manufacturer's data sheets for resistor values).

NOTES:

1. Address inputs A, B, C, D require 10 kΩ pull-up resistors.
2. The BFR 96 current source circuit may be replaced with an 820 Ω resistor to V_{EE}. This will result in a slight increase in insertion loss.
3. All capacitors are chip type, 0.1 µF/50 V.

Fig. 16 Test Jig 10x1

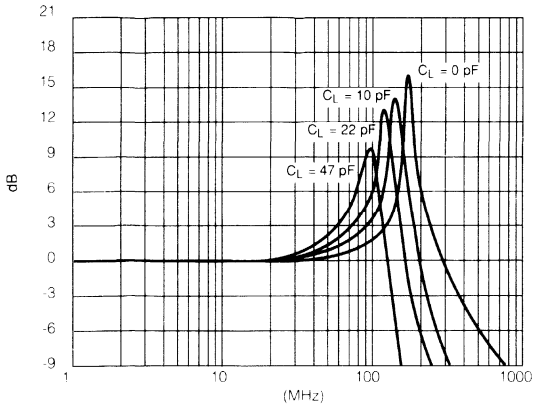


Fig. 17a Frequency Response 8x1

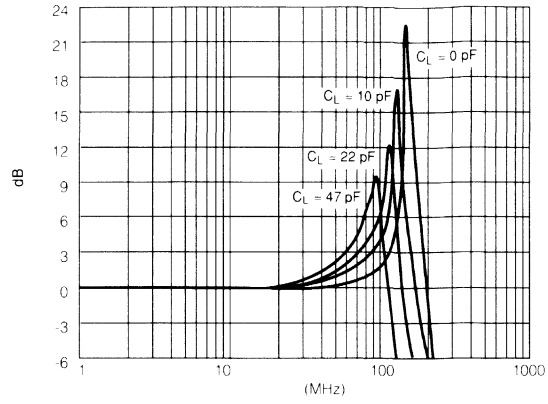


Fig. 17b Frequency Response 10x1

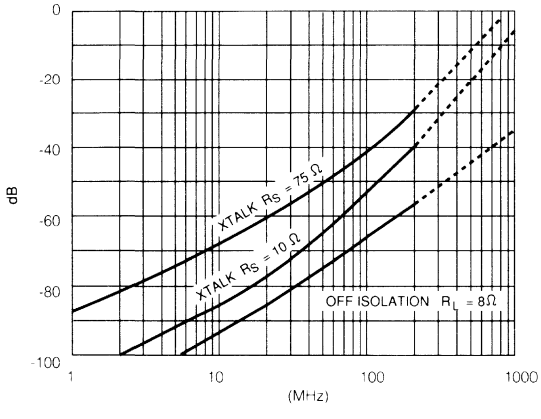


Fig. 17c Off-isolation and All Hostile Crosstalk 8x1

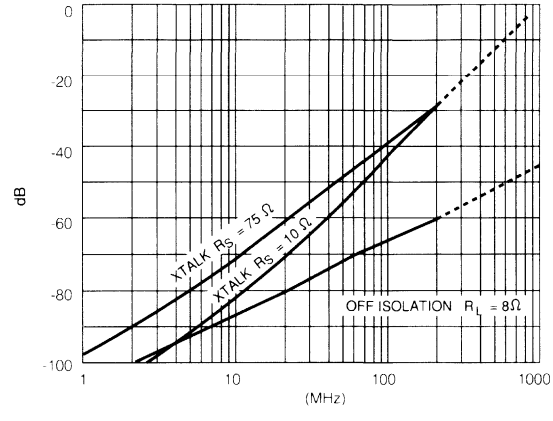


Fig. 17d Off-isolation and All Hostile Crosstalk 10x1

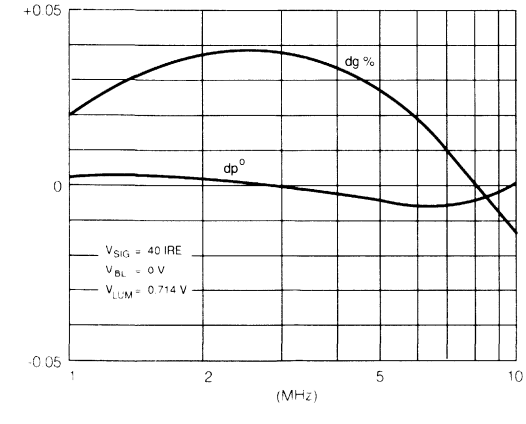


Fig.17e dg / dp vs frequency 8x1

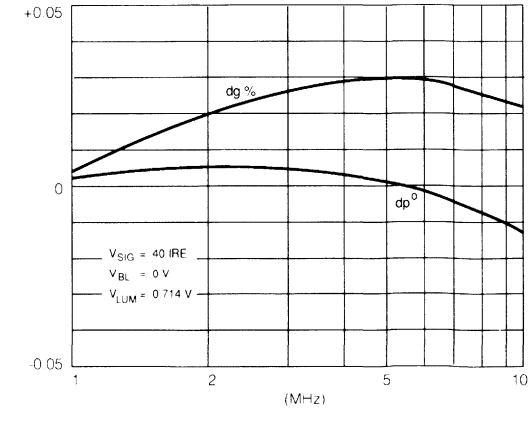


Fig.17f dg / dp vs frequency 10x1

APPLICATION CIRCUIT INFORMATION

Basic 8x1 and 10x1 video multiplexers can be implemented using circuits similar to the test jigs. Figures 18, and 19 show circuits of two other output buffers that can be used with the modules.

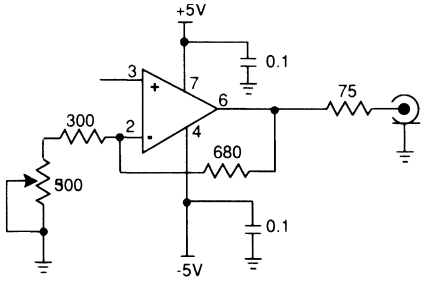


Fig.18 EL2030 Buffer Amplifier Circuit

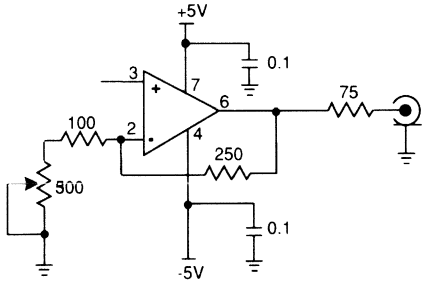


Fig. 19 CLC410 Buffer Amplifier Circuit

Both of them have exceptional differential gain and phase performance combined with a wide flat bandwidth. The gain of each amplifier was set to +6 dB in order to compensate for the loss through the combination of the 75 Ω back matching resistor and the 75 Ω load.

In both appliications, each VIDEO INPUT on the modules must be tied to ground with a low value resistance usually equal to the characteristic impedance of the input cable from the connector back plane. In this case the video can be either AC or DC coupled. In many applications however, DC restoration takes place before the signal goes into the cross-point switch.

The DC restorer quite often uses an operational amplifier at it's output. This amplifier can be tied directly to the VIDEO INPUT pin of the module without using a terminating resistor. A word of caution however, must be said at this point.

The internal circuitry of the GX4201 limits the useful input signal excursions. In a positive direction, the maximum voltage should not exceed +3 V and the negative excursion should not exceed -2 V. The device specifications indicate that the absolute maximum limits are +5.5 and -5.5 V.

It is important then, to never allow the output of any driver stage to exceed these limits. This may occur if one of the power supplies feeding the amplifier, fails. It is recommended that some form of clamping or protection is considered in these applications.

Since the VIDEO OUTPUT from the modules is high impedance when the module is disabled, it is very easy to connect one output to another to form a wider, n x 1 multiplexer.

It is possible with the modules described, to produce wider matrices for router cores. The 8x1 modules can be expanded to form, for example, 8x8 systems. Similarly, the 10x1 modules can be used to produce physically small sized 10x10 matrices.

Conclusions

The modules described in this application note can be used as stand-alone multiplexers for both NTSC/PAL broadcast and any HDTV format applications. In addition, by virtue of their size, their performance and the SIP pin outs, they may be used to form larger n x m, professional video matrices.

The high quality characteristics of the GX4201 devices assure virtually 'straight wire' performance of any video switcher in which they are used.

Additional information on the various crosspoint products manufactured by Gennum Corporation may be obtained from the Application Engineer of the Video Braodcast Products Group.

References

GENNUM Data Sheets:
GX4201 Video Crosspoint Switch
Document No. 510-74

GENNUM Application Notes:
Modular 16 x 1 Video Multiplexers
Document No. 510-85

Other Data Sheets:
EL2030: Elantec Incorporated
CLC110: Comlinear Corporation
CLC410: Comlinear Corporation
NE5539: Signetics Corporation.

Modular 16 x 1 Video Multiplexers

by Ian Ridpath, Senior Applications Engineer, Video and Broadcast Products Group

APPLICATION NOTE

INTRODUCTION

There are several important considerations that must be addressed when designing high performance video switching systems. These include the ease of input/output signal tracking, the ease of multiplexer expansion in order to form large routing matrices, system crosstalk and the repeatability of system parameters from channel to channel.

The modular multiplexers described in this application note, take these, as well as other points, into consideration and provide an optimal solution for the video design engineer. The 16x1 circuits are realised using four Gennum GX434 or GX214, 4x1 crosspoint ICs and two CMOS logic control ICs.

FUNCTIONAL DESCRIPTION

Figure 1 is a functional block diagram of the 16x1 module. The four 4x1 crosspoint ICs are multiplexed to form the 16x1 circuit. On-board chip select logic and enable logic is combined with a 4 bit latch in order to provide positive crosspoint selection. When the ENABLE line is HIGH, all crosspoint devices are disabled, producing a high impedance tri-state output.

Crosspoint selection is achieved by applying the appropriate four bit data to the address inputs, A0 through A3 and pulsing the STROBE input. When the STROBE is held LOW, the latches are transparent and the address data flows directly to the crosspoint devices. In this manner, synchronous switching is achieved by using both the ENABLE and STROBE inputs.

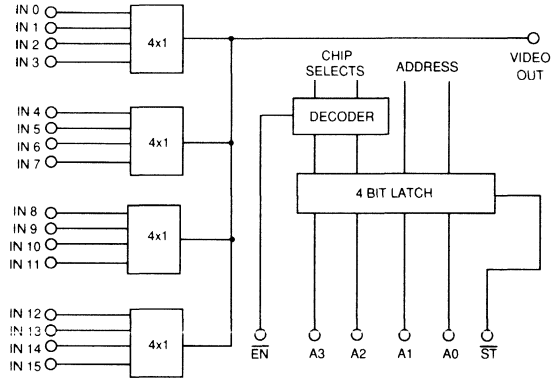


Figure 1

CIRCUIT DESCRIPTION (see Figure 2, page 2)

1. CROSSPOINT DEVICES

Each GX434 or GX214 device, (IC1 through IC4) is a 4x1 video multiplexer having on-chip address decoding, and chip select logic. The unilateral signal path consists of emitter followers at the input and output with level shifting circuits in between. Extremely high off-isolation is achieved by internal clamping in the signal path. The input impedance at each buffered input is extremely high, allowing for multi-input bussing.

The inputs may be directly driven from cables if a terminating resistor, equal to the characteristic impedance of the cable is connected from the input to ground.

The output requires a high impedance load of at least 10 kΩ to maintain the high degree of differential gain and phase characteristic of the crosspoint devices. The use of any number of high performance video buffers will allow the module to drive low impedance loads.

The device data sheets are available from Gennum Corporation (order document number 510-38 for the GX434 devices and document number 510-55 for the GX214 devices). They fully describe the operation of the devices along with electrical characteristics and performance curves.

2. LOGIC DEVICES

IC5 is a 74HC139, 2 to 4 decoder, selecting which of the four crosspoint devices is to be enabled.

A logical LOW from the decoder outputs is applied to the appropriate CHIP-SELECT input on each device.

Address bits A2 and A3 control the decoder so that only one output goes low for any of the four address possibilities. Selection of the four crosspoint switches within each crosspoint device is determined by the two address bits A0 and A1.

An ENABLE input on the 74HC139 is used to disable the decoder inputs, resulting in all the outputs going to a logic HIGH state. This causes all the GX4 outputs to go to their high impedance state, effectively disabling the module, simplifying the multiplexing of additional modules.

All address bits are latched by IC6, an MC4042 4-bit latch. This device has a STROBE input which can either be positive or negative acting. The polarity is determined by the logic level on pin 6. In this circuit application, pin 6 is tied to ground resulting in the latching action occuring on the STROBE transition from LOW to HIGH.

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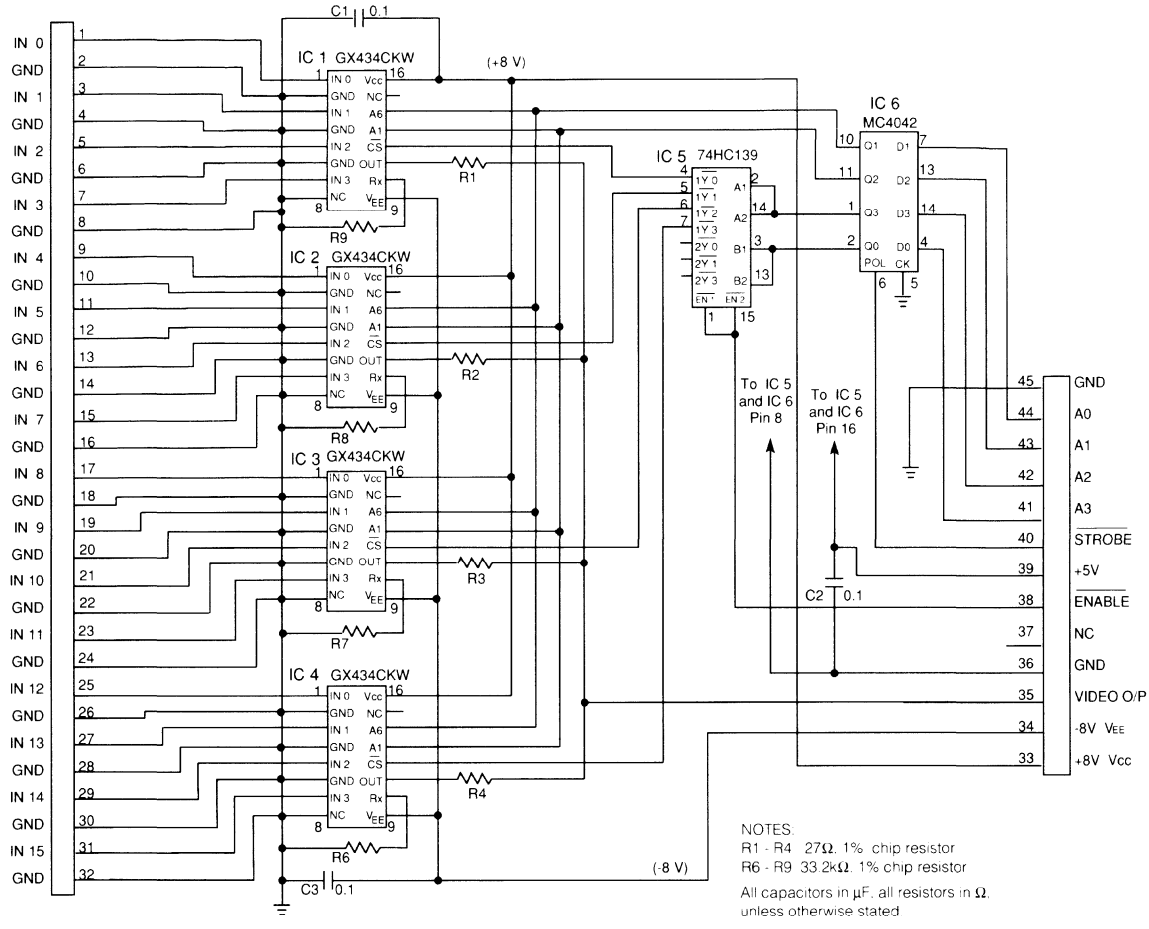


Fig. 2 16x1 Video Multiplexer Circuit

PIN CONNECTIONS

In designing this 16x1 video multiplexer, careful consideration was given to the assignment of pin connections. Figure 3 shows the resulting pin-outs. Each of the 16 inputs are separated by a ground pin in order to maintain a low degree of crosstalk.

The video output (pin 35), is separated from the inputs by the two crosspoint power supply pins. These supplies are normally ±8 V but can be as high as ±12 V.

The control logic inputs and the associated +5 V logic supply are all brought out at the opposite end of the video inputs. Inputs to other modules may be conveniently paralleled using this SIP format.

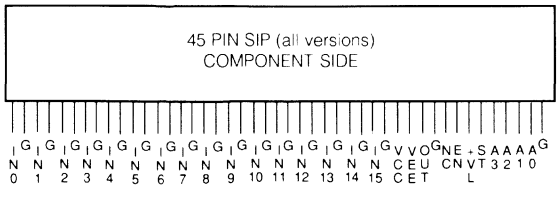


Figure 3

Key for Pin Connections

IN = video input	NC = no connection
G = ground	V_L = logic supply voltage
V_{CC} = positive supply voltage	EN = enable
V_{EE} = negative supply voltage	ST = strobe
Out = video output	A = address input

MODULE OPERATION

The Truth Table shown in Figure 4 describes the operation of the module. A logic HIGH on the $\overline{\text{ENABLE}}$ input overrides all other control inputs, resulting in the module being disabled and the video output going to a high impedance state. Thus,other module outputs may be directly interconnected to form an expanded multiplexer such as a 32x1 etc.

When the module is enabled with a logic LOW on the $\overline{\text{ENABLE}}$ input, the output reflects the latched input selected by ADDRESS BITS A0 through A3 when the $\overline{\text{STROBE}}$ input is returned from a logic LOW to a logic HIGH. Since each video input is represented by a high impedance, several inputs may be bussed to form multi-input matrices. It is important in these situations to carefully layout the motherboard using sufficient groundplane.

The bussed inputs should be driven from a stable, low impedance buffer amplifier. In some cases a small-value series resistor at each video input will prevent unwanted RF oscillations.

EN	ST	A3	A2	A1	A0	O/P
1	X	X	X	X	X	HI - Z
0	0	0	0	0	0	IN 0
0	0	0	0	0	1	IN 1
0	0	0	0	1	0	IN 2
0	0	0	0	1	1	IN 3
0	0	0	1	0	0	IN 4
0	0	0	1	0	1	IN 5
0	0	0	1	1	0	IN 6
0	0	0	1	1	1	IN 7
0	0	1	0	0	0	IN 8
0	0	1	0	0	1	IN 9
0	0	1	0	1	0	IN 10
0	0	1	0	1	1	IN 11
0	0	1	1	0	0	IN 12
0	0	1	1	0	1	IN 13
0	0	1	1	1	0	IN 14
0	0	1	1	1	1	IN 15
0	▲	X	X	X	X	latch state

X = don't care

Fig. 4 Truth Table

PRINTED CIRCUIT BOARD AND CIRCUIT OPTIONS

The printed circuit board may be either 0.0625in. or 0.03125in. thick glass-epoxy, double sided material with one ounce copper. Figure 5 shows the traces on the two sides of the board. All components are surface mounted except for the 45 input/output pins. They are 'finger' type leadframes and are soldered to both the component and 'copper' side of the board. Figure 6 details the component placement. When the GX434 devices are used, resistors R6 through R9 are included to set up currents in the devices in order to match the signal path delays from chip to chip. They are not needed on the GX214 devices and are replaced by a short circuit.

R1 through R4 are used at the output of each GX434 in order to flatten the frequency response. The GX214 does not use these resistors and they are replaced by a short circuit as well.

This produces frequency peaking which is a characteristic ofthe crosspoint devices. In this case, the frequency response is flattened by using the roll-off characteristics of the external output buffer to compensate the natural peaking of the cross-points.

As well, R1 through R4 may be omitted on the GX 434 version and replaced with short circuits. Again this will result in frequency peaking but now at a high amplitude and at a higher frequency. This may be easily compensated, as before, by the external buffer but now producing an even wider bandwidth flat response.

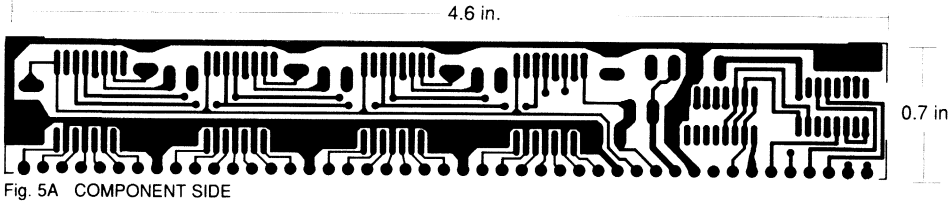


Fig. 5A COMPONENT SIDE

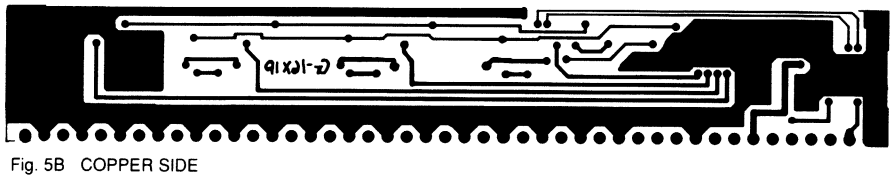


Fig. 5B COPPER SIDE

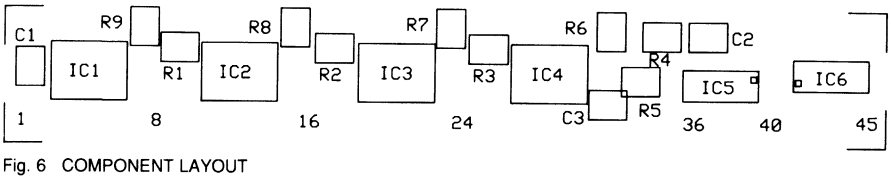


Fig. 6 COMPONENT LAYOUT

TESTING AND PERFORMANCE EVALUATION

Once the assembly of the modules is complete, the task of testing and evaluating the performance can be achieved using a suitable test jig.

The jig should itself be constructed using careful R.F. design techniques for the video signal paths. Suitable power supply
decoupling capacitors should be used for each of the three supplies. Address selection can be made using toggle, DIP or decoded thumbwheel switches. Each one of the logic inputs
requires a 10k Ω pull-up resistor.

Critical measurements of differential gain and phase can be done using a wideband network analyser such as the Hewlett Packard 4195A. A video vectorscope can also be used but will result in a less accuate measurement.

As far as the frequency response is concerned, the network analyser can be used to produce extremely accurate results. The advantage of using a network analyser such as the 4195A is that a hardcopy plot may be obtained for any measurement made. Also, the measurement set-up data can be stored for repeated tests.

Figure 7 shows the circuit of the test jig used in the lab at Gennum.

The buffer amplifier shown is an NE5539 ultra wideband operational amplifier. Other amplifiers, such as the Elantec EL2030 as well as the VTC VA708 have been used and have given similar results. (It should be remembered that the signal path is initially normalised before measurements are taken with the network analyser).

In order to measure off-isolation and all hostile crosstalk, of the module itself, the inputs must be extremely well shielded and careful attention must be paid to lead dress. When using the network analyser, the measurements involve applying a +15 dBm signal to the OFF switch in order to maintain the noise floor below 100 dB. This level must be reduced to -20 dBm for tests on ON switches.

The following graphs are typical results obtained from measuring 15 engineering prototypes. Both the GX434 and GX214 modules were tested using the same jig. The GX214 version requires an external 1500 resistor from the Video O/P to V_{EE}.

Note: This current source is internal on the GX434 devices. Also, the 1500 Ω resistor (R5) can be mounted as a chip resistor on the GX214 module itself if no other modules, with their own resistors, are to be paralleled.

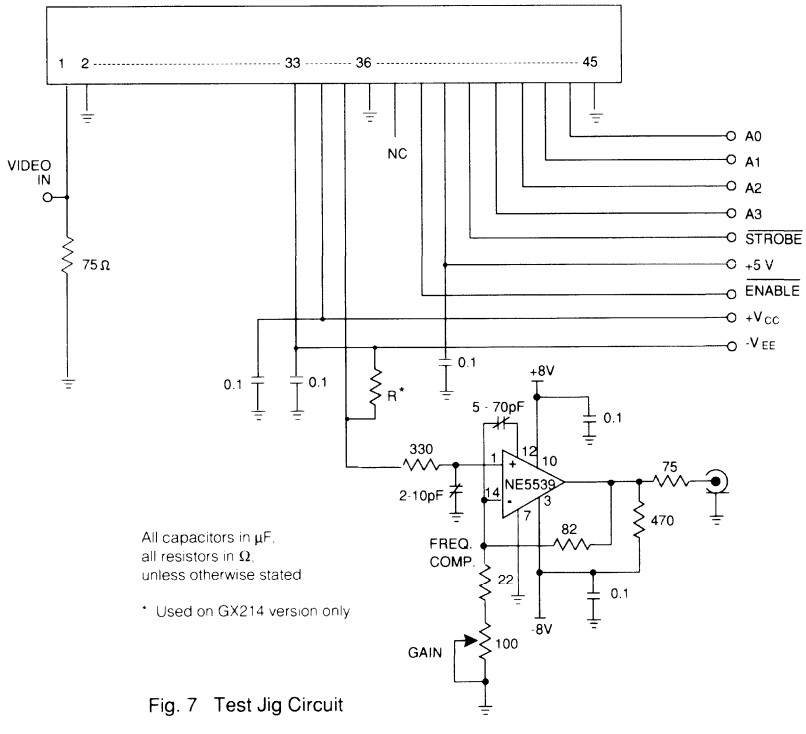


Fig. 7 Test Jig Circuit

Fig. 8 Typical Test Results for the GX434 and GX214 Modular 16x1 Multiplexer

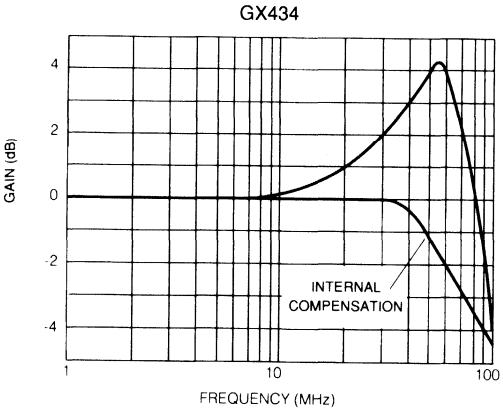


Fig. 8A

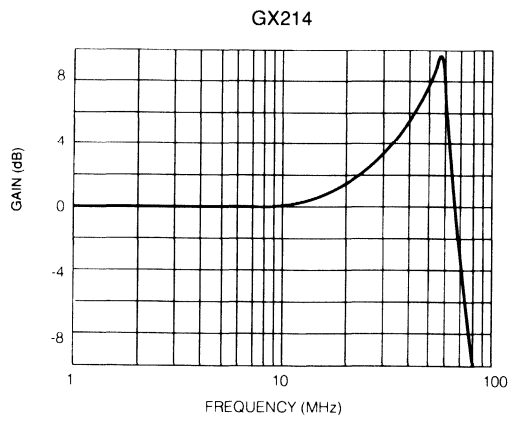


Fig. 8B

Frequency Response

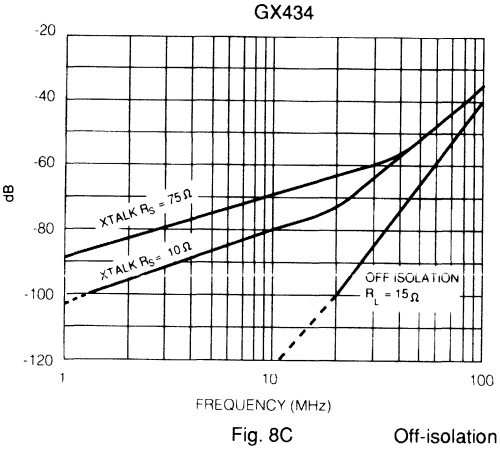


Fig. 8C

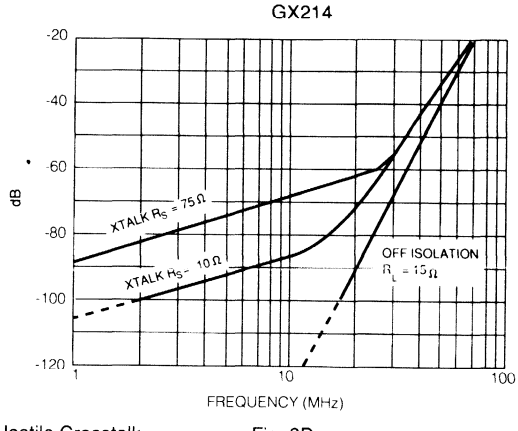


Fig. 8D

Off-isolation and All Hostile Crosstalk

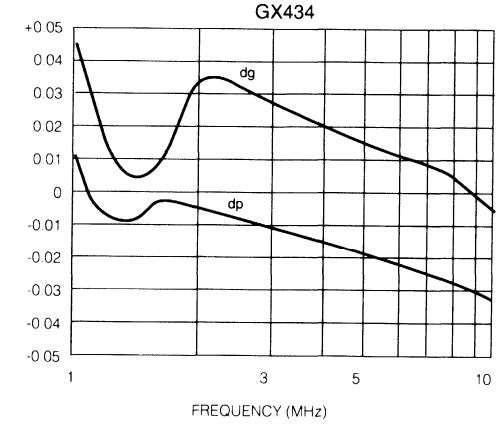


Fig. 8E

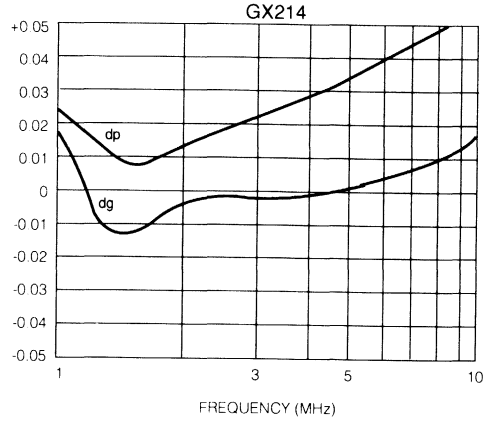


Fig. 8F

Differential Gain and Phase

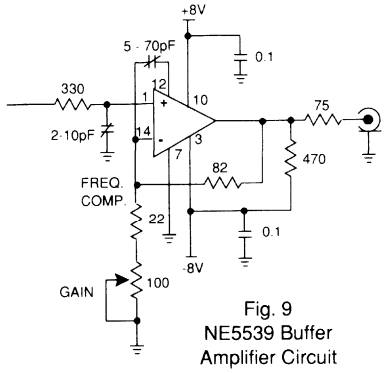


Fig. 9
NE5539 Buffer
Amplifier Circuit

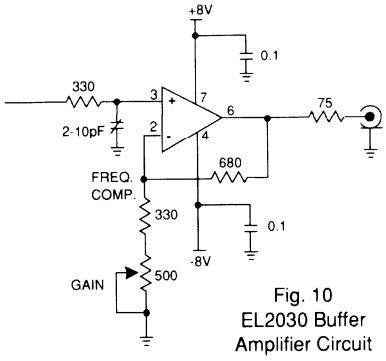


Fig. 10
EL2030 Buffer
Amplifier Circuit

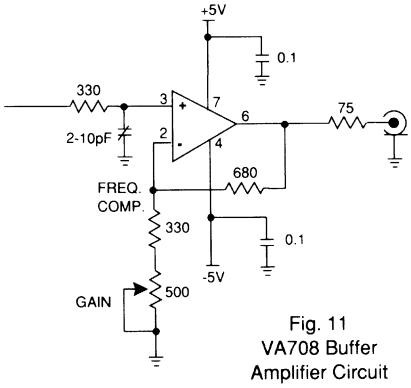


Fig. 11
VA708 Buffer
Amplifier Circuit

APPLICATION CIRCUITS AND INFORMATION

A basic 16x1 video multiplexer can be implemented using a circuit similar to the test jig shown in Figure 7. Figures 9 , 10 and 11 show circuits of the three different output buffers used to evaluate the module. All of them have good differential gain and phase performance combined with a wide flat bandwidth. The gain of each amplifier was set to +6 dB in order to compensate for the loss through the combination of the 75 Ω back matching resistor and the75 Ω load.

In this 16x1 application, each VIDEO INPUT must be tied to ground with a low value resistance, usually equal to the characteristic impedance of the input cable from the connector back plane. In this case the video can be either AC or DC coupled.

In many applications however, DC restoration takes place before the signal goes into the crosspoint switch.

The DC restorer quite often has an op-amp at its output. This amplifier can be tied directly to the VIDEO INPUT pin of the module without using a terminating resistor.

A word of caution must be said at this point. The internal circuitry of the GX434 limits the useful input signal excursions. In a positive direction, the maximum voltage should not exceed +2 V and the negative excursion should not exceed -1.2 volts. The device specifications indicate that the absolute maximum limits are +2.4 and -4 volts. It is important then, to never allow the output of any driver stage to exceed these limits. This may occur if one of the power supplies feeding the amplifier, fails. It is recommended that some form of clamping or protection is considered in these applications

The situation for the GX214 devices is not as critical since the maximum positive signal excursion is +5 V. The maximum negative excursion remains the same.

One solution is to clamp the video at the output rather than at the input. The variation in DC offset from one crosspoint to another in the module is only ±7 mV, centred around +7 mV for the GX434 version.

The DC offset for the GX214 module is much wider, ranging from -45 to -120 mV. Thus, output DC clamping is imperative.

Since the VIDEO OUTPUT from the modules is high impedance when the module is disabled, it is very easy to connect one output to another to form a wider, n x1 multiplexer.

Figure 12 shows a 32 x1 set-up using two modules. A few points are worth mentioning when multiplexing additional modules.

The typical output capacitance of the GX434 module is 60 pF. The same parameter for the GX214 module is 48 pF. Therefore, any additional module connected to the output bus will add the amount of capacitance mentioned.

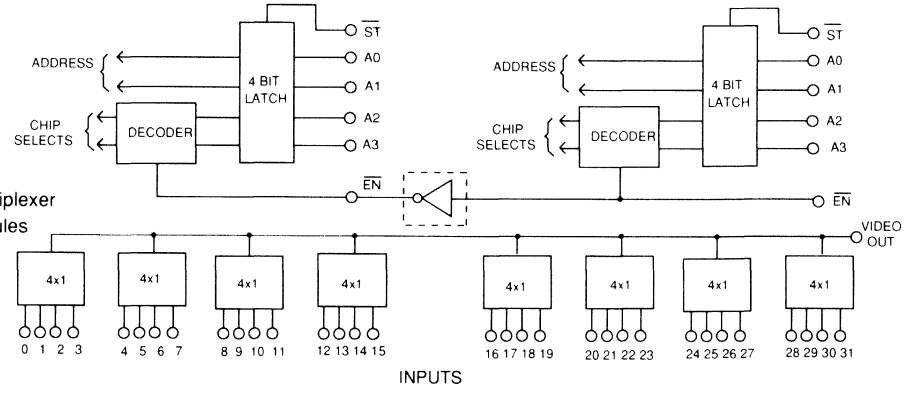


Fig. 12 32 x1 Multiplexer using Two Modules

Since the amount of peaking in an emitter-follower is affected by the load capacitance, any other modules on the output will alter the new system frequency response. If no on-board frequency peaking compensation is included on the modules, then the final frequency response can still be tailored by the roll-off frequency response of the output amplifier.

For the compensated GX434 module, this cannot be done. The 27 Ω on-board resistors that were used at the output of each GX434 device, were chosen to flatten the response while the module was driving a high impedance buffer amplifier with virtually no input capacitance.

Now, however, if an extra 60 pF is connected to the output, the response will roll-off at a much lower frequency. It is recommeneded that the on-board resistors be removed from the GX434 module when it is to be used as part of a wider nx1 multiplexer system.

On the other hand, when the modules are to be used in a 16 x n matricies, the above problem does not occur because each output is from only one module. The only problems that may occur for wide-input matricies are, the possibility of instability due to poor input driver performance, or, long input cable or lead lengths.

As mentioned before, this problem can usually be overcome by adding a small series resistor (100 Ω max.) as close as possible to each input.

The convenient SIP pin-outs on the module mean that all inputs can be easily paralleled from one module to another. As long as sufficient groundplane is provided along the input bus paths, these modules may be used in wide input/output matricies. A practical example would be a 16x16 system.

In this case, module selection would be controlled from a microprocessor using the $\overline{\text{ENABLE}}$ and $\overline{\text{STROBE}}$ inputs with appropriate buffering and data latching.

It is possible with the modules described, to produce a 16 x16 router core with dimensions. of only 5 x 7 inches, excluding input/output buffers and logic.

CONCLUSIONS

The modules described in this application note can be used as stand-alone multiplexers for both broadcast and CCTV applications. In addition, by virtue of their size, performance and SIP pin outs, they may be used to form larger n x m, professional video matrices.

Additional information on the various crosspoint products manufactured by Gennum Corporation maybe obtained from the Application Engineer of the Video and Broadcast Products Group.

References

GENNUM Data Sheets:

GX434: Document No. 510-38

GX214: Document No. 510-55

GENNUM Application Notes:

Frequency Peaking Compensation:

Document No. 510-39

16 x 1 Video Crosspoint EvaluationBoard;

Document No. 510-48

Other Data Sheets:

EL2030: Elantec Incorporated

VA708: VTC Corporation

NE5539: Signetics Corporation.

POWER SUPPLY CONTROLLERS

RESONANT MODE

PULSE WIDTH MODULATION

GENNUM CORPORATION

Resonant Mode Power Supply Controller

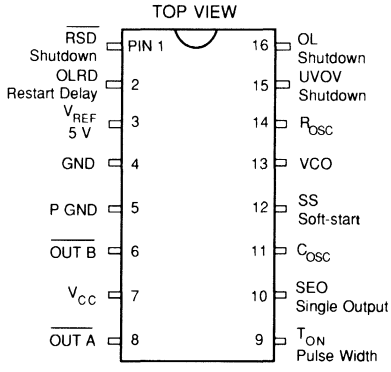
GP605 DATA SHEET

FEATURES

- frequency range of 1 kHz to 2 MHz
- operating frequency range (min. and max.) set by a resistor and a capacitor
- pulse width set by a resistor and capacitor
- synchronous overload shutdown with delayed restart
- synchronous overvoltage, undervoltage and remote shutdown
- soft-start
- single-ended or complementary outputs
- drives power MOSFETs directly (0.8 A peak)
- low cost 16 pin DIP or SOIC

ABSOLUTE MAXIMUM RATINGS

Parameter	Value & Units
Supply Voltage	20 V
Undervoltage/Overvoltage Input	-0.4 V - 6 V
Overload Input	-0.4 V - 6 V
Remote Shutdown	-0.4 V - V_{CC}
VCO Input	-0.4 V - V_{CC}
Storage Temperature	-65°C ≤ T_S ≤ 150°C
Lead Temperature (soldering, 10 sec.)	260°C
Junction Temperature	150°C
Power dissipation at T_A ≤ 70°C (derate 9 mW/°C for T_A > 70°C)	720 mW



PIN CONNECTION
16 PIN DIP

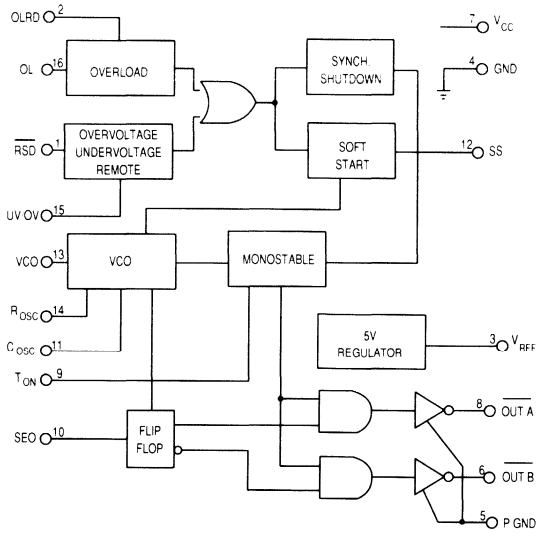
CIRCUIT DESCRIPTION

The GP605 utilizes frequency modulation instead of pulse width modulation to achieve regulation. The pulse width is held constant while the frequency is varied over an operating range set by a resistor and capacitor. A feedback voltage controls the switching frequency of the two complementary outputs, which are capable of driving power MOSFETs directly.

Opening a normally grounded control pin puts the GP605 into single-ended operation. In this mode the frequency is doubled and the two outputs are identical so they can be paralleled for increased drive capability.

The high operating frequency of up to 2 MHz results in significant reductions in the size of the required magnetic and capacitive components in the power supply. This leads to dramatic savings in volume, weight and manufacturing cost of switching power supplies.

Included on the chip are peripheral functions such as soft-start, undervoltage/overvoltage lockout, remote shutdown and overload shutdown with delayed restart. All shutdown modes are synchronous (the last output pulse is completed), and default to soft-start once the fault condition is removed.



FUNCTIONAL BLOCK DIAGRAM

Document No. 510 - 43 - 3

GENNUM CORPORATION P.O. Box 489, Stn A, Burlington, Ontario, Canada L7R 3Y3 tel. (416) 632-2996 fax: (416) 632-2055 telex: 061-8525
Japan Branch: 301 Aoba Building, 3-6-2 Takanawa, Minato-ku, Tokyo 108, Japan tel. (03) 441-2096 fax: (03) 448-8991

ELECTRICAL CHARACTERISTICS

Limits apply over $0°C \le T_A \le 70°C$ for the GP605CDC and GP605CKC
$-25°C \le T_A \le 85°C$ for the GP605IDC and GP605IKC
and $-55°C \le T_A \le 125°C$ for the GP605MDC

Parameters tested on open loop test circuit
Typical values are at $T_A = 25°C$
* Parameters marked with an asterisk * are valid only at $T_A = 25°C$
$V_{CC} = 12V$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Chip Supply					
Supply Voltage		10	12	20	V
Internal V_{CC} Undervoltage Threshold		8.5	9.0	9.5	V
Threshold Hysteresis		-	5	-	%
Supply Current *	Undervoltage condition	18	22	24	mA
Voltage Control Oscillator					
Maximum Frequency	Single output Complementary output	- -	2 1	- -	MHz MHz
Tolerance of f_{MAX} * Tolerance of f_{MIN} *	Fig. 6 Fig. 5	- -	- -	±5 ±20	% %
Temperature coefficient f_{MAX} Temperature coefficient f_{MIN}		300 400	600 700	-900 1000	ppm/°C ppm/°C
Dead Time T_{OFF} *		-	200	300	ns
Operating Range of VCO Input (Pin 13)	MAX MIN	- -	6.5 1.1	- -	V V
Linearity of the VCO		-	-	±5	%
Internal Pull-up Resistor (Pin 13) *		9.6	12	14.4	kΩ
Output Pulse Width T_{ON} Tolerance *		-	-	±5	%
Temperature Coefficient of T_{ON}		0	400	800	ppm/°C
Output Section					
Output Risetime Output Falltime	100pF ‖ 100kΩ load on OUT A, OUT B	- -	20 15	40 30	n sec n sec
Output Mismatch	$\overline{\text{OUT A}}$ & $\overline{\text{OUT B}}$: Pin 10 SEO open	-	5	25	n sec
Output Low Level (sink) *	$\overline{\text{OUT A}}$ vs $\overline{\text{OUT B}}$ 20 mA 200 mA	- -	- -	0.7 2.7	V V
Output High Level (source) *	$\overline{\text{OUT A}}$ & $\overline{\text{OUT B}}$ -20 mA -200 mA	V_{CC} -2.5 V_{CC} -2.8	- -	- -	V V
Reference Section					
Output Voltage *		4.75	5.00	5.25	V
Temperature Stability		-200	100	300	ppm/°C
Max Current Capability		-	10	-	mA

ELECTRICAL CHARACTERISTICS continued

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Shutdown Section					
Soft-start * (1)	C_S = 2.2 µF, VCO = 7 V	16	19	22	ms
Overload Restart Delay	2R = 330 kΩ, C = 6.8 µF	1.0	1.3	1.6	sec
Propagation Delay to Shutdown (2)		-	200	300	n sec
Remote Shutdown (3)	Enabled	V_{CC} -0.8	-	-	V
	Disabled	-	-	3	V
Overload Shutdown (OL) Threshold *		2.84	3.0	3.16	V
OL Threshold Temp. Coefficient		-400	100	500	ppm/°C
OL Hysteresis		-	3	-	%
OL Trigger Pulse Width		500	-	-	n sec
OL Input current Range		-1	-	+15	µA
Overvoltage Threshold Lockout *			2.84	3.0	3.16 V
Undervoltage Threshold Lockout *		1.8	1.9	2	V
Temp. Coeff. of Thresh'd Voltage		-400	100	500	ppm/°C
Hysteresis of the Lockout Voltage		-	3	-	%
Input Current Range (Pin 15)		-1	-	+22	µA

Thermal Impedance	16 pin DIL Plastic Package θ JC	-	42	-	°C/W
	16 pin DIL Plastic Package θ CA	-	70	-	°C/W
	16 Pin SOIC θ JA	-	112	-	°C/W

NOTE:

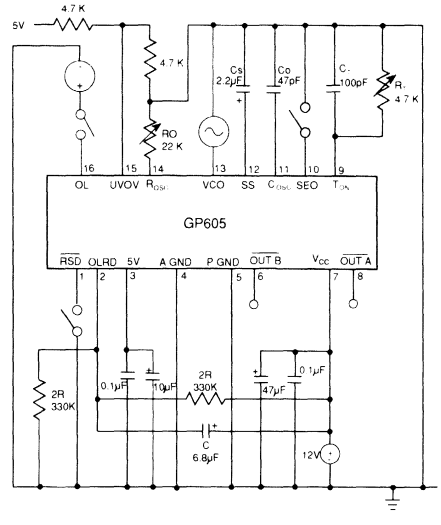
(1) Soft-start time is measured from output enable at minimum frequency to time at which maximum frequency is reached.

(2) If the shutdown input is triggered 200 ns before the next output pulse is expected, there will be no pulses. If there is a pulse earlier than 200 ns, this pulse is completed in full before the output is disabled. This is known as synchronous shutdown, a necessary feature in any resonant mode controller.

(3) Refer to pin description for current required.

Part Number (10 digits)	Package Type	Temperature Range
GP605--CDC	16 Pin DIP	0° to 70° C
GP605--CKC	16 Pin SOIC	0° to70° C
GP605--IDC	16 Pin DIP	-25° to 85° C
GP605--IKC	16 Pin SOIC	-25° to 85° C
GP605--MDC	16 Pin DIP	-55° to 125° C

ORDERING INFORMATION



OPEN LOOP TEST CIRCUIT

3-3

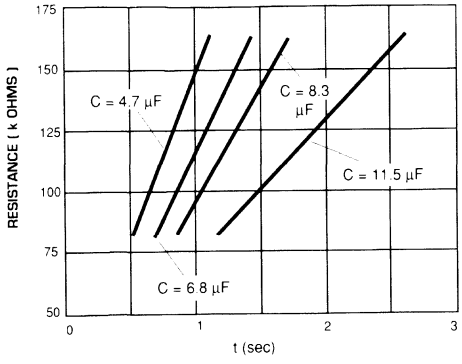


Fig. 1 Overload Restart Delay

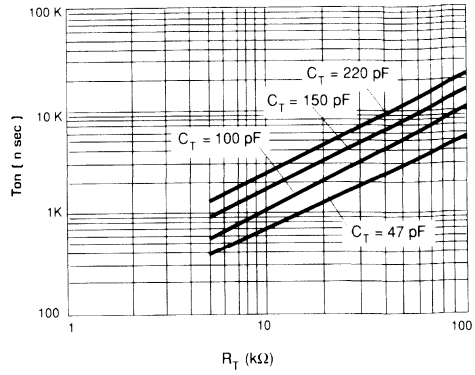


Fig. 2 Output Pulse Width

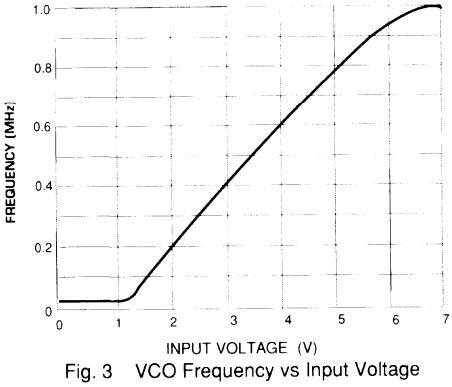


Fig. 3 VCO Frequency vs Input Voltage

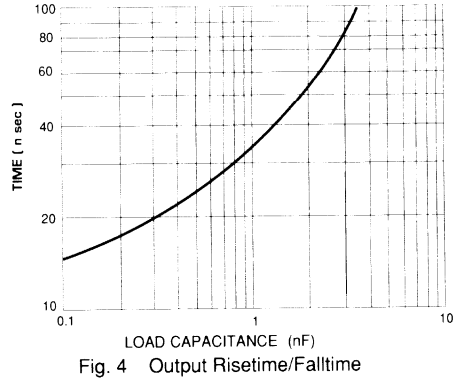


Fig. 4 Output Risetime/Falltime

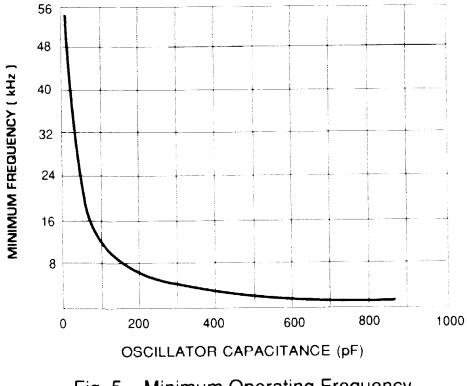


Fig. 5 Minimum Operating Frequency

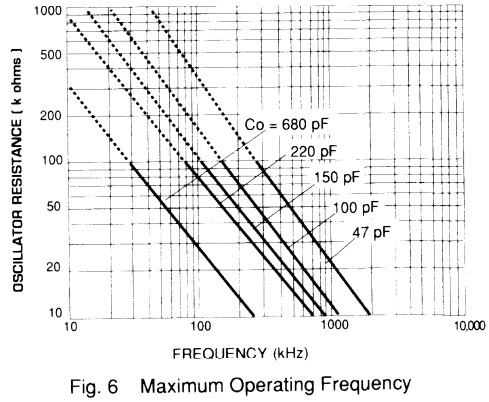


Fig. 6 Maximum Operating Frequency

TYPICAL PERFORMANCE CURVES OF THE GP605

For all graphs, V_{CC} = +12 VDC and T_A = 25 °C. The curves shown above represent typical batch sampled results.

PIN FUNCTIONS

The GP605 is a complex device, so the best place to start is with a functional pin description.

Pin 1 (*RSD*) - Remote Shutdown
A low on pin 1 shuts down the GP605. When the pin is released the GP605 goes into soft-start. This pin is normally driven by an open collector transistor where the current is given by:

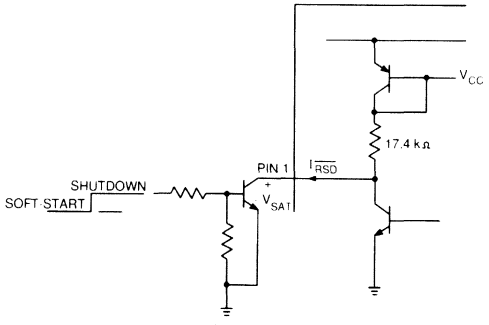


Fig. 7

$$I_{RSD} = \frac{(V_{CC} - V_{SAT} - 0.7)}{17.4\ k\Omega}\ mA \pm 20\%$$

For CMOS or bipolar circuitry, the configuration may be:

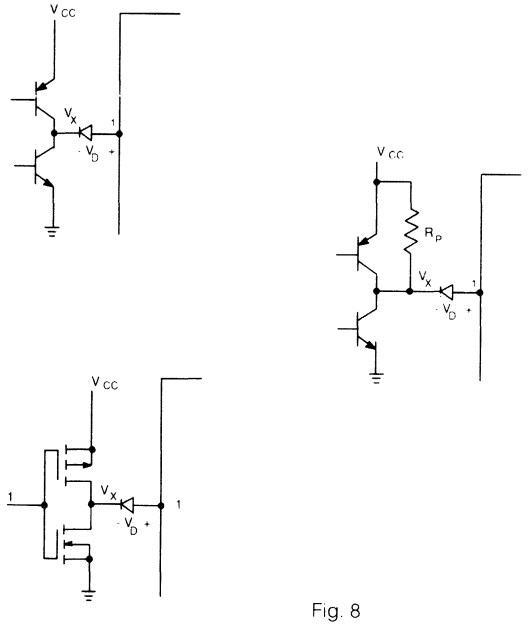


Fig. 8

In all cases the voltage must pull up to a minimum of

$$V_X = V_{CC} - 0.8\ V$$

assuming diode voltage $V_D \approx 0.4$ V when it is off (non-conducting). If remote shutdown is not used, leave pin 1 open.

Pin 2 (*OLRD*) - Overload Restart Delay
A 330 kΩ + 330 kΩ voltage divider in combination with a 6.8 µF capacitor generates a 1.3 second shutdown to restart delay every time the overload sense (pin 16) is activated. Timing starts when the overload is removed; upon timeout soft-start begins. Refer to Figure 1 to select RC combinations for other delays.

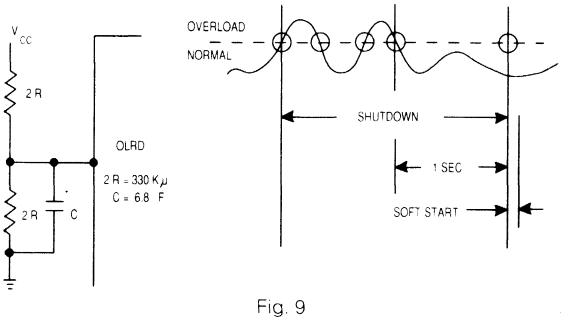


Fig. 9

Pin 3 (*5V*) - 5V Reference
This is a 5% tolerance regulator used to power most of the internal circuitry. To improve noise rejection it is recommended to decouple this pin with a 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor.

Pin 3 can be used as a reference for any external circuitry as long as the load is less than 10 mA.

Pin 4 (*GND*) - Analog Ground
Great care must be taken to ensure that grounds are run so that any voltage drops from high ground currents are minimized and do not interfere with feedback voltages and the reference.

Pin 5 (*P GND*) - Power Ground
Only the output transistors are connected to the power ground, to minimize interference with the logic circuitry.

GND and P GND are to be connected outside the package, with the decoupling of the supply to this point.

Pin 6 (*OUT B*) - Output B
Output B is an active low output driver, where the low duration (pulse width) is T_{ON}. It is complementary to pin 8 ($\overline{OUT\ A}$). For proper operation, the voltage on the output pins must not go below ground potential or above V_{CC} by more than 0.5 volts.

Pin 7 (V_{CC}) - Supply Voltage
The power supply trace must be decoupled as close to pin 7 as possible. Currents of 0.5 A levels may be drawn by the GP605. Minimum recommended decoupling is with a 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor.

Pin 8 ($\overline{OUT\ A}$) - Output A
Output A is an active low output driver, where the low duration (pulse width) is T_{ON}, and is complementary to pin 6.

Pin 9 (T_{ON}) - Pulse Width

The constant pulse width T_{ON} is set by a resistor R_T and capacitor C_T. This relationship is shown in Figure 2. $R_T \times C_T$ should have a temperature coefficient of -500 ppm/°C for best stability and fall within the following ranges:

$$5\ k\Omega \leq R_T \leq \text{no limit}$$
$$47\ pF \leq C_T \leq 100\ nF$$

The R_T and C_T should be connected as close as possible to GND to minimize ground noise variations. The upper limit on pulse width is determined by chip-to-chip variation, power supply and component tolerances. The worst case combination must give $T_{ON} < 1/f_{MAX} - T_{OFF}$, where $T_{OFF} = 200$ ns typ. (300 ns max.). The off period is required by the design of the GP605. The pulse width T_{ON} should be set to give an off period greater than T_{OFF} so that the circuit will operate correctly at f_{MAX}, where f is the actual operating frequency. Rewriting the equation as:

$$T_{OFF} = 1/f - T_{ON}$$

The GP605 will divide the output frequency by two when T_{OFF} decreases to 200 ns. This is a failsafe feature to ensure the pulse width will never be incorrect by limiting f_{MAX}. Under normal operation f_{MAX} should be limited using R_{OSC}.

Pin 10 (*SEO*) - Single Ended Output

This pin is normally grounded for complementary outputs in push-pull applications. Opening pin 10 results in a single ended output at double the frequency. $\overline{OUT A}$ and $\overline{OUT B}$ can then be shorted together for increased drive capability.

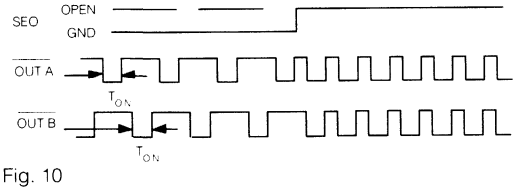


Fig. 10

Pin 11 (C_{OSC}) - Oscillator Capacitor

The capacitor C_{OSC} on this pin, controls the minimum frequency f_{MIN} of the VCO operating range. Refer to Figure 5 for selection. Layout is critical for this component, keeping leads as short as possible and connecting close to the A GND pin.

Pin 12 (*SS*) - Soft-Start

A capacitor C_S on this pin provides a controlled start up from $f$min to f_{MAX}. The delay is approximately $T_{TS}(ms) \approx 8.7\ C_S(\mu F)$ for C_S between zero and 47 µF.

To ensure a full soft-start duration when soft-start is caused by an undervoltage or overvoltage fault, it is necessary to have the fault present for about half the soft-start time.

Pin 13 (*VCO*) - Voltage Controlled Oscillator Input

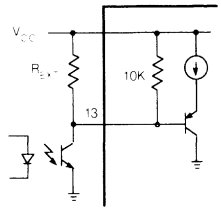


Fig. 11

The VCO input is designed for an optocoupler feedback network from the secondary (output) side of the power supply. An internal 10 kΩ pull-up resistor is provided but an external resistor may be used if a lower value is required. The control characteristic is shown in Figure 3. The linear input range is from 1.1 V to 6.5 V where 1.1 V represents $f$min and 6.5 V represents f_{MAX}.

Pin 14 (R_{OSC}) - Oscillator Resistor

The resistor R_{OSC} on this pin, controls f_{MAX}, the maximum frequency of the VCO operating range. C_{OSC} the capacitor controlling f_{MIN} must be selected first, then refer to Figure 6 for selection of R_{OSC}. For good stability, a 1% resistor with a temperature coefficient of -600 ppm/°C, is recommended. Minimum value for R_{OSC} is 10 kΩ.

Pin 15 (*UVOV*) - Undervoltage/Overvoltage

The input is a window comparator. A higher or lower voltage than the thresholds specified will shut down the power supply until voltage falls within the window again, at which point the GP605 goes into soft-start. If pin 15 is not used, it must be tied to V_{CC} or the 5 V reference via a voltage divider, generating a bias voltage, which falls within the window. The voltage divider should carry approximately 1 mA. The maximum input voltage on this pin is 6 V.

Pin 16 (*OL*) - Overload Input

A voltage exceeding the specified threshold on this pin will cause the GP605 to shut down and activate the overload restart delay function. This delay starts when the input voltage drops below the threshold. On time-out, soft-start begins. The maximum input voltage on this pin is 6 V. If pin 16 is not used, short it to ground. No capacitor is required on pin 2 (ORLD), but a bias voltage between $V_{CC}/3$ and $V_{CC}/3 + 5.7$ V is still needed. A convenient voltage is $V_{CC}/2$.

A TYPICAL APPLICATION CONFIGURATION

Figure 12 shows the GP605 as a resonant mode power supply providing 5 VDC output. L_R and C_R form the series resonant tank. V_{CC} is generated locally for high efficiency, using a start-up circuit which is biased off after V_{CC} stabilises. T2 senses the current in the primary of T3 and provides the overload signal.

For more information, request Application Notes 510-62 and 510-63.

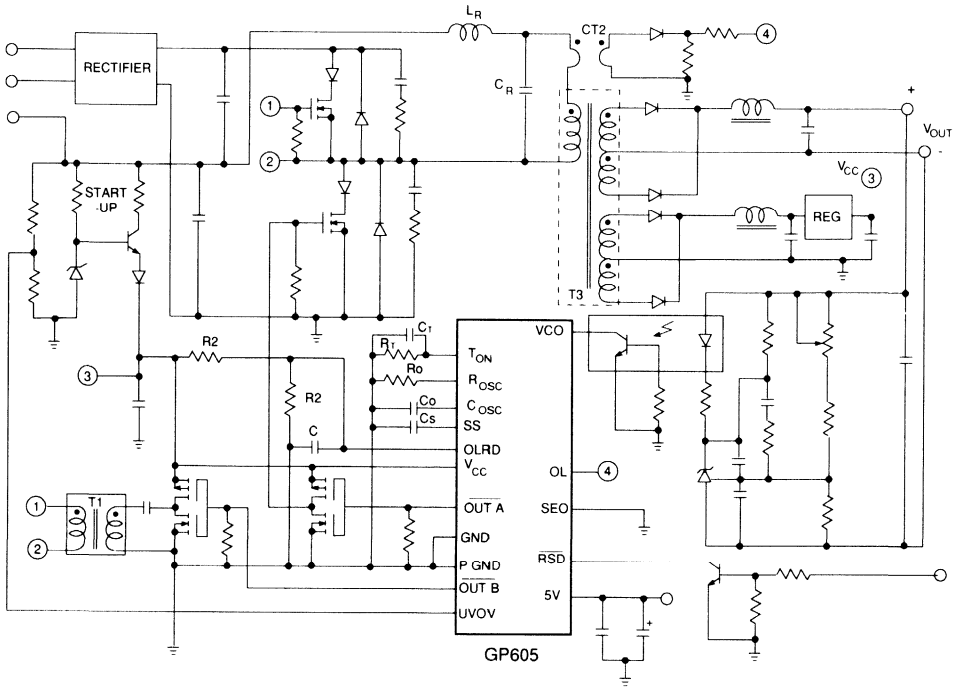


Fig. 12 Typical GP605 Application

AVAILABLE PACKAGING

16 pin DIP 16 pin SOIC

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

GENNUM CORPORATION

Single-ended ZCS Resonant Mode Power Supply Controllers

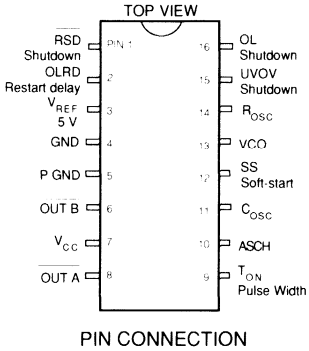
GP6040 and GP6041 PRELIMINARY DATA SHEET

FEATURES

- frequency range of 1 kHz to 3 MHz
- operating frequency range set by a resistor (max.) and a capacitor (min.)
- pulse width set by a resistor and capacitor
- low start-up current
- synchronous overload shutdown with delayed soft restart
- synchronous overvoltage, undervoltage and remote shutdown
- asynchronous shutdown
- soft-start
- single-ended output
- drives power MOSFETs directly (1.6 A peak)
- low cost 16 pin DIP or SOIC

ABSOLUTE MAXIMUM RATINGS

Parameter	Value & Units
Supply Voltage	20 V
Undervoltage/Overvoltage Input	-0.4 V - 6 V
Overload Input	-0.4 V - 6 V
Remote Shutdown	-0.4 V - V_{CC}
VCO Input	-0.4 V - V_{CC}
Storage Temperature	-65°C ≤ T_S ≤ 150°C
Lead Temperature (soldering, 10 sec.)	260°C
Junction Temperature	150°C
Power dissipation at T_A ≤ 70°C	720 mW
(derate 9 mW /°C for T_A > 70°C)	



PIN CONNECTION
16 PIN DIP

CIRCUIT DESCRIPTION

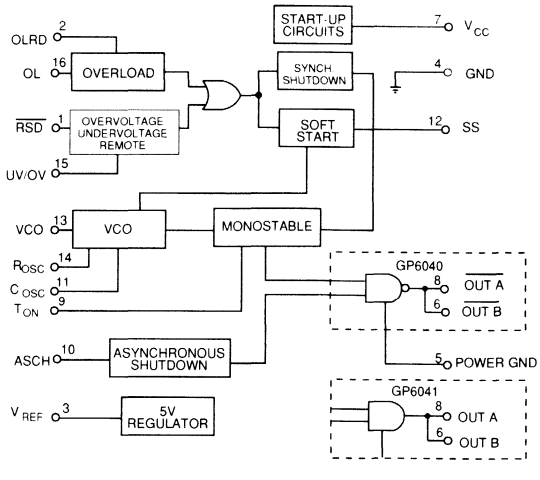
The GP6040 and GP6041 are highly reliable, single-ended, resonant mode power supply controllers. These devices support zero current switch (ZCS) resonant and quasi-resonant topologies operating in variable frequency mode. The pulse width is held constant while the frequency is varied by a feedback voltage over an operating range. Maximum and minimum frequency is set by an external resistor and capacitor. Fixed pulse width is adjust-ed by an external RC network.

The single totem pole output has a 1.6 A peak current capability. The GP6040 provides active low driver output. The GP6041 provides active high driver output.

The high operating frequency of up to 3 MHz results in significant reductions in EMI noise and minimizes the size of the required magnetic and capacitive components in the power supply.

Included on the chip are peripheral functions such as soft-start, undervoltage/overvoltage lockout, remote shutdown and overload shutdown with delayed restart. All shutdown modes are synchronous (the last output pulse is completed), and default to soft-start once the fault condition is removed. The asynchronous shutdown provides emergency OFF for catastrophic failures. The controller also contains power supply undervoltage lockout, minimizing supply current during the start-up condition.

The GP6040 and GP6041 are upgraded single-ended, pin-to-pin compatible versions of the GP605. The controller has been design optimized to support zero current switching topologies.



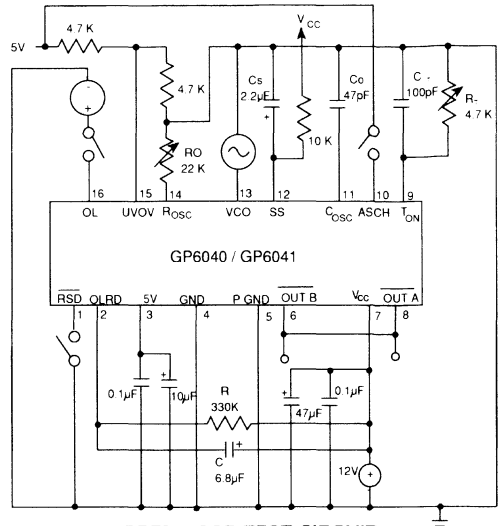
FUNCTIONAL BLOCK DIAGRAM

3-9

GENNUM CORPORATION P.O. Box 489, Stn A, Burlington, Ontario, Canada L7R 3Y3 tel. (416) 632-2996 fax: (416) 632-2055 telex: 061-8525
JAPAN BRANCH: 301 Aoba Building, 3-6-2, Minato-ku, Tokyo 108, Japan tel. (03) 441-2096 fax: (03) 448-8991

Part Number (10 digits)	Package Type	Temperature Range
GP6040-CDC GP6041-CDC	16 Pin DIP	0° to 70° C
GP6040-CKC GP6041-CKC	16 Pin SOIC	0° to 70° C
GP6040-EDC GP6041-EDC	16 Pin DIP	-40° to 85° C
GP6040-EKC GP6041-EKC	16 Pin SOIC	-40° to 85° C
GP6040-MDC GP6041-MDC	16 Pin DIP	-55° to 125° C

ORDERING INFORMATION



OPEN LOOP TEST CIRCUIT

ELECTRICAL CHARACTERISTICS

Limits apply over
- 0°C ≤ T_A ≤ 70°C for the GP6040/41CDC, and GP6040/41CKC
- -40°C ≤ T_A ≤ 85°C for the GP6040/41EDC, and GP6040/41EKC
- -55°C ≤ T_A ≤ 125°C for the GP6040/41MDC

Parameters tested on open loop test circuit
Typical values are at T_A = 25°C
★ Parameters marked with an asterisk* are valid only at T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Chip Supply					
Supply Voltage		10	12	20	V
Chip Enable V_{CC} Threshold *		-	13.0	-	V
V_{CC} Undervoltage Lockout *		-	9.0	-	V
Supply Current	V_{CC} = 11 V (UV condition) V_{CC} = 12 V	- 18	2 24	5 26	mA mA
Voltage Control Oscillator					
Maximum Frequency		2.4	3	-	MHz
Tolerance of f_{MAX} * Tolerance of f_{MIN} *	C_O = 100 pF V_{VCO} = 10 V R_O = 12 kΩ V_{VCO} = 0 V	- -	- -	±5 ±20	% %
Temperature coefficient f_{MAX} Temperature coefficient f_{MIN}	R_O = 12 kΩ C_O = 100 pF R_T = 4.7 kΩ C_T = 100 pF	-400 600	-700 900	-900 1100	ppm/°C ppm/°C
Dead Time T_{OFF} *		-	90	-	ns
Operating Range of VCO Input (Pin 13) (Pin 13)	max min	- -	6.5 1.1	- -	V V
Internal Pull-up Resistor (Pin 13) *		9.6	12	14.4	kΩ
Output Pulse Width T_{ON} Tolerance *	R_T = 4.7 kΩ C_T = 100 pF	-	-	±5	%
Temperature Coefficient of T_{ON}	T_{ON} = 500 ns GP6040	-	-200	-	ppm/°C
	GP6041	-	-780	-	ppm/°C

ELECTRICAL CHARACTERISTICS continued

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Section					
Output Risetime	100pF II 100 kΩ load on O_{UT}	-	10	30	ns
Output Falltime	(See Fig. 7)	-	10	30	ns
Output Low Level (sink)*	$I_{OUT\ B}$ = 20mA	-	-	0.7	V
	$I_{OUT\ B}$ = 200mA	-	-	2.2	V
Output High Level (source)*	$I_{OUT\ B}$ = -20mA	V_{CC}-2.0	-	-	V
	$I_{OUT\ B}$ = -200mA	V_{CC}-2.2	-	-	V
Reference Section					
Output Voltage*	I_{REF} = 10 mA	4.75	5.00	5.25	V
Temperature Stability		-200	100	300	ppm/°C
Maximum Current Capability		-	10	-	mA
Shutdown Section					
Prop. Delay to Sync. Shutdown (1)			-	300	400 ns
Remote Shutdown Trigger Level	Enabled	Vcc -0.8	-	-	V
	Disabled	-	-	3	V
Remote Shutdown Current Trigger*		-	250	-	µA
Overload Shutdown (OL) Threshold*		3.04	3.2	3.36	V
OL Threshold Temp. Coefficient		-400	100	500	ppm/°C
OL Hysteresis		-	3	-	%
OL Trigger Pulse Width		500	-	-	ns
OL Input Current Range (Pin 16)		-1	-	+15	µA
Overvoltage Threshold* Lockout		3.04	3.2	3.36	V
Undervoltage Threshold* Lockout		-	1.9	2.0	V
Temp. Coeff. of Thresh'd Voltage		-400	100	500	ppm/°C
Hysteresis of the Lockout Voltage		-	4	-	%
Input Current Range (Pin 15)		-1	-	+22	µA
Propogation Delay to Asynchronous Shutdown* (ASCH)		-	70	100	ns
ASCH Threshold Lockout*		3.32	3.5	3.68	V
Input Current Range (Pin 10)		-1	-	+22	µA
Thermal Impedance	16 pin DIL Plastic Pack. q JC	-	42	-	°C/W
	16 pin DIL Plastic Pack. q CA	-	70	-	°C/W
	16 Pin SOIC q JA	_	112	-	°C/W

NOTES

(1) If the shutdown input is triggered 200 ns (typ) or earlier (e.g. 300 ns) before the next output pulse is expected, there will be no pulses. If the shutdown input is triggered between 200 ns and the time the output pulse is on the output pin, this pulse will be completed in full before the output is disabled.

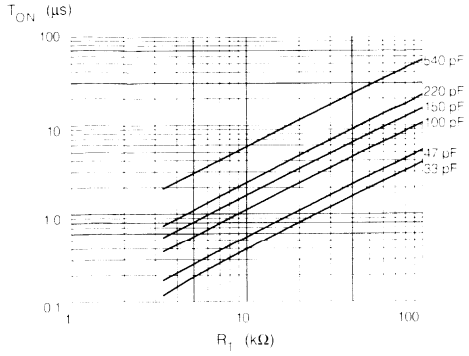


Fig. 1 Output Pulse Width GP6040

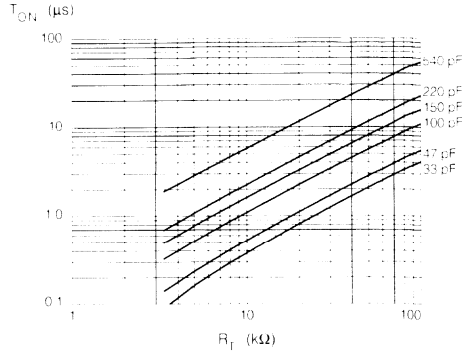


Fig. 2 Output Pulse Width GP6041

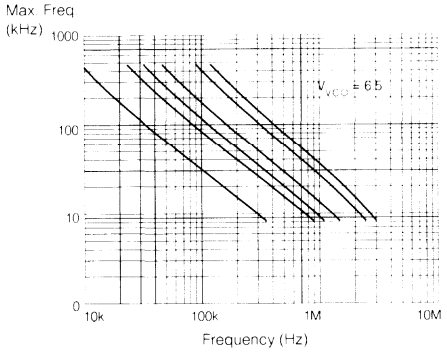


Fig. 3 Maximum Operating Frequency GP6040/41

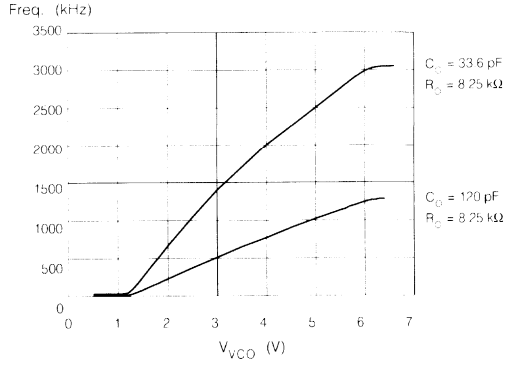


Fig. 4 VCO Frequency vs Input Voltage GP6040 / 41

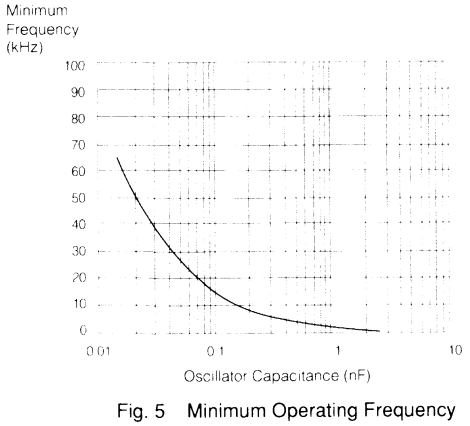


Fig. 5 Minimum Operating Frequency GP6040/41

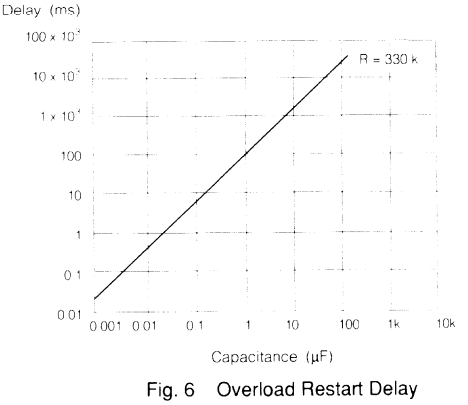


Fig. 6 Overload Restart Delay GP6040/41

TYPICAL PERFORMANCE CURVES OF THE GP6040 AND GP6041

For all graphs, *Vcc* = +12 volts DC and T_A = 25 °C. The curves shown above represent typical batch sampled results.

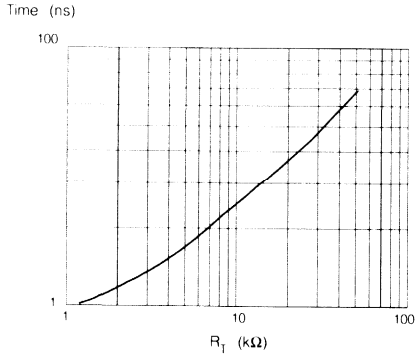


Fig. 7 Output Risetime/Falltime GP6040/41

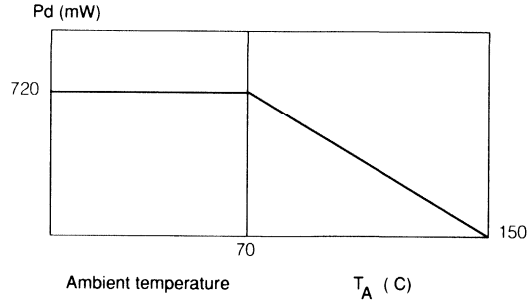


Fig. 8

PIN FUNCTIONS

Pin 1 (RSD) - Remote Shutdown

A low level (or in current mode - high sink current) on Pin1 synchronously shuts down the GP6040 or GP6041. When the pin is released (in current mode - zero current), the controller goes to soft-start. If remote shutdown is not used, leave Pin 1 open. In Fig. 9 the simplified remote shut down internal circuit is shown.

The transistors T1 and T2 constitute the current mirror. To activate shutdown it is necessary to source from the GP6040 or GP6041 current I_{RSD} = 250 µA (min). The ability to choose between current or voltage mode shutdown allows for operation in a noisy environment. Figure 10 shows some sample applications for the shutdown external circuits.

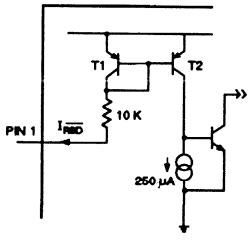


Figure 9

Pin 2 (OLRD) - Overload Restart Delay

This input sets the overload restart delay if pin 16 (Overload sense) is activated. Timing starts when the overload is removed; upon time-out, soft-start begins. Refer to Fig. 6 to select proper value of the capacitor. Recommended value of the bias resistor is 330kΩ. For overload restart delay time it makes no difference if the capacitor is connected to the ground or to the V_{CC} line. However if the capacitor is connected to the ground, during initial power up condition, the soft-start will be delayed by the time equal to the overload restart delay time. If the capacitor is connected to the V_{CC} line, soft-start follows only 1ms internal delay time (necessary to stabilise +5V reference line).

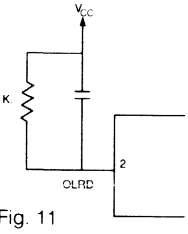


Fig. 11

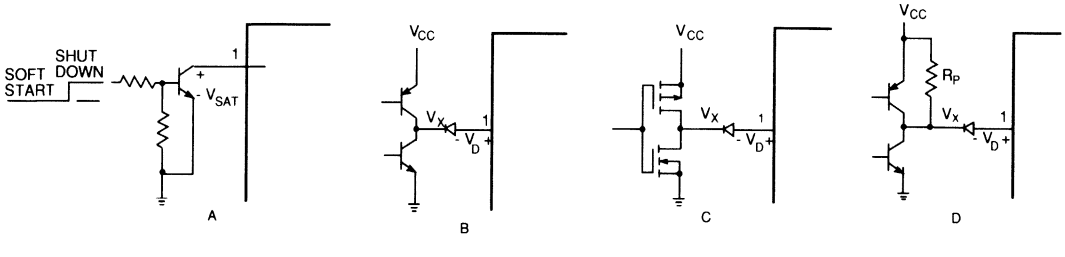


Figure 10

Pin 3 (V_{REF}) - +5V Reference

The 5% tolerance regulator is used to power most of the internal circuity. It can be used as a reference for external circuity as long as the load is less than 10mA. For a 1% tolerance regulator contact Gennum's Power Products Department.

To improve noise rejection ratio it is recommended to decouple pin 3 to the logic ground with a 2.2 µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor.

Pin 4 (GND) - Ground

Great care must be taken to ensure that grounds are run so that any voltage drops from high ground currents are minimised and do not interfere with feedback voltages and references.

Pin 5 (PGND) - Power Ground

Only the output transistor should be connected to the power ground, to minimize interference with the logic circuity. GND and PGND are to be connected outside the package. The connection point should be carefully chosen and decoupled.

Pin 6 (OUT B) - Output B

The GP6040 provides an active low fixed pulse width output. The GP6041 provides an active high fixed pulse width output. For the risetime and falltime characteristics refer to Fig.7.

Pin 7 (V_{CC}) - Supply Voltage

The power supply trace must be decoupled as close to pin 7 as possible. Currents of 1.6A levels may be drawn by the GP6040 and GP6041. Minimum recommended decoupling is 10 µF tantalum capacitor in parallel with 0.1 µF ceramic capacitor.

The controller is equipped with a low startup current circuit. The hysteresis is adjusted as follow: turn on at 13 V (typ) and synchronous turn off if the voltage drops to 9 V (typ). The threshold voltage of the hysteresis was chosen to make controller compatible to its predecessor GP605. If different threshold voltages are required contact Gennum's Power Products Department.

Pin 8 (OUTA) - Output A

This output has all basic characteristics identical to the Output B (pin 6) but is connected into it through a 1.5Ω (±10%) serial resistor. Such a configuration allows for eliminating the series resistor in some applications. It is still possible to join Output A and Output B together.

Pin 9 (T_{ON}) - Pulse Width

The constant pulse width T_{ON} is set by a resistor R_T andcapacitor C_T. This relationship is shown in Fig.1 for GP6040 and Fig. 2 for GP6041. $R_T \times C_T$ should have a temperature coefficient of +200 ppm/°C (GP6040) and +750 ppm/°C (GP6041) for best stability. The T_{ON} time is generated by a monostable multivibrator and may have any required duration. The only limit is the minimum value of the resistor $R_T \geq 3.3\ k\Omega$ due to the current capability of the pin 9. The monostable works in re-triggerable mode. It means that if the maximum frequency set by external components is higher than specified in description of the pin 14, the T_{ON} time remains constant, however the frequency will divide by two. This feature could be used as an inherent current limit. Under normal operation f_{MAX} should be clamped by proper choice of the resistor R_{OSC}.

Pin 10 (ASCH) - Asynchronous Shutdown

This input is added in place of the single-ended input used on the GP605. In zero current switching topology it may prevent transistor damage in some catastrophic failures (eg. short output diode). The triggering level of the asynchronous shutdown is set in such a way that it is possible to use it simultaneously with the overload sense circuit.

In ZCS topology ASCH input is meant to be used in emergency situations only. There are two ways to reset the asynchronous shutdown. By disconnecting the V_{CC} line or by forcing pin 10 to the level below 0.5V. The release of the asynchronous shutdown does not provide any of the soft-start features. For soft-start options, connect pin 10 to either the OVUV or OL synchronous shutdown pins. The reset function is not available on early release devices marked "PRE" on the top of the package.

Pin 11 (C_{OSC}) - Oscillator Capacitor

The capacitor on this pin, C_O, controls the minimum frequency f_{MIN} of the VCO operating range. The capacitor C_O, must be selected as the first component of the oscillator section. Refer to Fig. 5 for selection. For good stability a capacitor with a temperature coefficient of -750 ppm/°C is recommended.

Pin 12 (SS) - Soft-Start

A capacitor C_{SS} on this pin provides a controlled start-up from f_{MIN} to the frequency set by the VCO input. The delay is approximately $t_{SS} \approx 0.6 \times R_{SS} \times C_{SS}$

where Css - soft start capacitor

Rss - external resistor (if resistor not used R = 5.1 M 20%)

The value of the C_{SS} is not limited. To ensure a full soft-start after UVOV fault, it is necessary to have the fault present for half the soft-start time (to ensure discharge of the C_{SS} capacitor).

Pin 13 (VCO) - Voltage Controlled Oscillator Input

The VCO input is designed for an optocoupler feedback network from the secondary (output) side of the power supply. An internal 10 kΩ (typ.) pull-up resistor is provided but an external resistor may be used if a lower value is required. The control characteristic is shown in Fig. 4 .

Pin 14 (R_{OSC}) - Oscillator Resistor

The resistor on this pin, R_O, controls f_{MAX}, the maximum frequency of the VCO operating range. Refer to Fig. 3 for

selection of R_O. This resistor should be selected after C_O was chosen. The use of a 1%, zero temperature coefficient resistor is recommended for good stability. Minimum value for R_O is 8.2 kΩ. For normal operation the maximum frequency should be set no higher than:

$$f_{MAX} \leq \frac{1}{T_{ON} + T_{DT}}$$

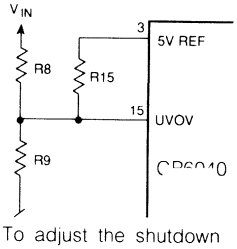
where T_{ON} - constant pulse width

T_{DT} - dead time specified in the data sheet.

If this requirement is not fulfilled the controller divides the output frequency by two.

Pin 15 (UVOV) - Undervoltage/Overvoltage Shutdown

This input is a window comparator. A higher or lower voltage than the thresholds specified will synchronously shutdown the power supply until the input voltage falls within the window again, at which point the GP6040 or GP6041 goes into Soft-Start. If Pin 15 is not used, it must be tied to V_{CC} via a voltage divider generating a bias voltage which falls within the window. The maximum input voltage on this pin is 6V. To adjust the shutdown hysteresis levels use an additional resistor connected to the +5V line.



The value of the resistors can be calculated from the equations:

$$R15 = \frac{(V_o \times V_r) - (V_u \times V_r)}{(V_u \times V_{ino}) - (V_o \times V_{inu})} \times R8$$

$$R9 = \frac{R8 \times V_r \times (V_o - V_u)}{V_r \times (V_{ino} - V_{inu} + V_u - V_o) + (V_o \times V_{inu} - V_u \times V_{ino})}$$

where V_o - the GP6040/41 overvoltage threshold lockout

V_u - the GP6040/41 undervoltage threshold lockout

V_r - reference voltage

V_{ino} - requested line overvoltage lockout

V_{inu} - requested line undervoltage lockout

Pin 16 (OL) - Overload Input

A voltage exceeding the specified threshold on this pin will cause the GP6040 or GP6041 to synchronously shutdown and activate the overload restart delay function. This delay starts when the input voltage drops below the threshold. On time-out Soft-Start begins. The maximum input voltage on this pin is 6V. If Pin 16 is not used, short it to ground.

AVAILABLE PACKAGING
16 PIN DIP AND 16 PIN SOIC

CAUTION
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SENSITIVE DEVICES
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GENNUM CORPORATION

Resonant Mode Power Supply Controllers

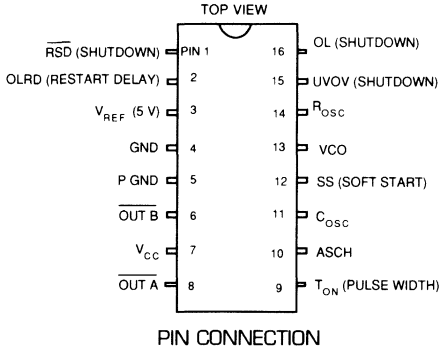
GP6050 and GP6051 TENTATIVE DATA SHEET

FEATURES

- frequency range of 1 kHz to 3 MHz
- operating frequency range set by a resistor (max.) and a capacitor (min.)
- pulse width set by a resistor and capacitor
- low start-up current
- synchronous overload shutdown with delayed soft restart
- synchronous overvoltage, undervoltage and remote shutdown
- soft-start
- complementary outputs
- drives power MOSFETs directly (0.8 A peak)
- low cost 16 pin DIP or SOIC

ABSOLUTE MAXIMUM RATINGS

Parameter	Value & Units
Supply Voltage	20 V
Undervoltage/Overvoltage Input	-0.4 V - 6 V
Overload Input	-0.4 V - 6 V
Remote Shutdown	-0.4 V - V_{CC}
VCO Input	-0.4 V - V_{CC}
Storage Temperature	-65°C ≤ T_S ≤ 150°C
Lead Temperature (soldering, 10 sec)	260°C
Junction Temperature	150°C
Power dissipation at T_A ≤ 70°C	720 mW
(derate 9 mW /°C for T_A > 70°C)	



PIN CONNECTION
16 PIN DIP

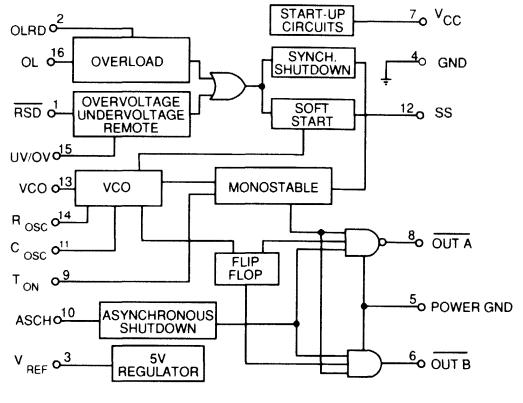
CIRCUIT DESCRIPTION

The GP6050 and GP6051 are highly reliable, complementary output, resonant mode power supply controllers. The GP6050 is an upgraded, pin-to-pin compatible version of the GP605. The GP6051 provides an inverted driver output with respect to the GP6050. These devices support resonant and quasi-resonant topologies operating in variable frequency mode. To achieve regulation the pulse width is held constant while the frequency is varied by a feedback voltage over an operating range. Maximum and minimum frequency is set by an external resistor and capacitor. Fixed pulse width is adjusted by an external RC network.

The complementary totem pole outputs have 0.8 A peak current capability. The GP6050 provides active low driver output. The GP6051 provides active high driver output.

The high operating frequency of up to 3 MHz results in significant reductions in EMI noise and minimizes the size of the required magnetic and capacitive components in the power supply.

Included on the chip are peripheral functions such as soft-start, undervoltage/overvoltage lockout, remote shutdown and overload shutdown with delayed restart. All but one shutdown modes are synchronous (the last output pulse is completed), and default to soft-start once the fault condition is removed. The controller also contains power supply undervoltage lock-out, minimizing supply current during the start-up condition.



FUNCTIONAL BLOCK DIAGRAM

Document No. 510 - 58 - 2

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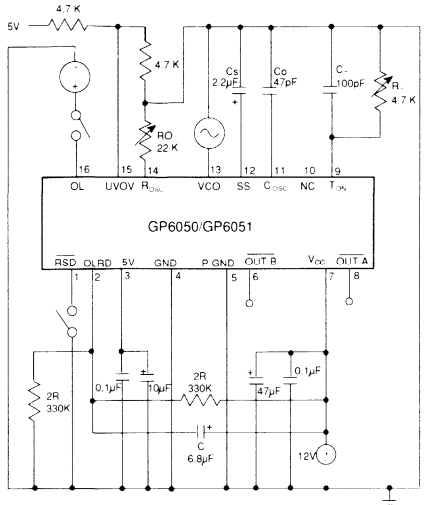

OPEN LOOP TEST CIRCUIT

AVAILABLE PACKAGING

16 pin DIP 16 pin SOIC

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EXCEPT AT A STATIC-FREE WORKSTATION

ELECTRICAL CHARACTERISTICS

Parameters tested on open loop test circuit Typical values are at T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Chip Supply					
Supply Voltage		10	12	20	V
Chip Enable V_{CC} Threshold		-	11	-	V
V_{CC} Under Voltage Lockout		8.5	9.0	9.5	V
Supply Current	Undervoltage condition Normal condition	- 18	5 22	- 24	mA mA
Voltage Control Oscillator					
Maximum Frequency	Single output Complementary output	2.4 1.2	3 1.5	- -	MHz MHz
Tolerance of f_{MAX} Tolerance of f_{MIN}	Fig. 6 Fig. 5	- -	- -	±5 ±20	% %
Temperature coefficient f_{MAX} Temperature coefficient f_{MIN}		-300 400	-600 700	-900 1000	ppm/°C ppm/°C
Dead Time T_{OFF}		-	100	125	ns
Operating Range of VCO Input (Pin 13)	MAX MIN	- -	6.5 1.1	- -	V V
Linearity of the VCO		-	-	±5	%
Internal Pull-up Resistor (Pin 13)		9.6	12	14.4	kΩ
Output Pulse Width T_{ON} Tolerance		-	-	±5	%
Temperature Coefficient of T_{ON}		0	400	800	ppm/°C

ELECTRICAL CHARACTERISTICS continued

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Section					
Output Risetime	100pF II 100kΩ load on	-	20	40	n sec
Output Falltime	$\overline{OUT A}$, $\overline{OUT B}$	-	15	30	n sec
Output Mismatch	$\overline{OUT A}$ & $\overline{OUT B}$, Pin 10 SEO open	-	5	25	n sec
Output Low Level (sink)	$\overline{OUT A}$ vs $\overline{OUT B}$ 20mA	-	-	0.7	V
	200mA	-	-	2.2	V
Output High Level (source)	$\overline{OUT A}$ & $\overline{OUT B}$ -20mA	-	-	V_{CC}-2	V
	-200mA	-	-	V_{CC} -2.2	V
Reference Section					
Output Voltage		4.75	5.00	5.25	V
Temperature Stability		-200	100	300	ppm/°C
Max Current Capability		-	10	-	mA
Shutdown Section					
Soft-start (1)	C_S = 2.2 µF, VCO = 7V	16	19	22	ms
Overload Restart Delay	2R = 330 kΩ, C = 6.8 µF	1.0	1.3	1.6	sec
Propagation Delay to Shutdown (3)		-	200	300	n sec
Remote Shutdown (2)	Enabled	V_{CC} -0.8	-	-	V
	Disabled	-	-	3	V
Overload Shutdown (OL) Threshold		2.84	3.0	3.16	V
OL Threshold Temp. Coefficient		-400	100	500	ppm/°C
OL Hysteresis		-	3	-	%
OL Trigger Pulse Width		500	-	-	n sec
OL Input current Range		-1	-	+15	µA
Overvoltage Threshold Lockout		2.84	3.0	3.16	V
Undervoltage Threshold Lockout		1.8	1.9	2.0	V
Temp. Coeff. of Thresh'd Voltage		-400	100	500	ppm/°C
Hysteresis of the Lockout Voltage		-	3	-	%
Input Current Range (Pin 15)		-1	-	+22	µA
Thermal Impedance	16 pin DIL Plastic Package θ JC	-	42	-	°C/W
	16 pin DIL Plastic Package θ CA	-	70	-	°C/W
	16 Pin SOIC θ JA	-	112	-	°C/W

NOTES

Revision Date April 1990

(1) Soft-start time is measured from output enable at minimum frequency to time at which maximum frequency is reached.

(2) Refer to pin description for current required.

(3) If the shutdown input is triggered 200 ns before the next output pulse is expected, there will be no pulses. If there is a pulse earlier than 200 ns, this pulse is completed in full before the output is disabled.
This is known as synchronous shutdown, a necessary feature in any resonant mode controller.

GENNUM CORPORATION

Single-ended ZVS Resonant Mode Power Supply Controllers

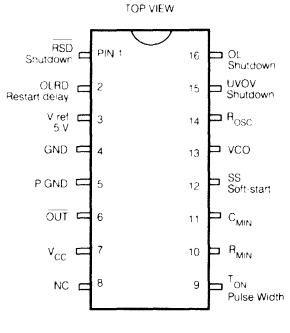
GP6140 and GP6141 PRELIMINARY DATA SHEET

FEATURES

- frequency range of 1 kHz to 3 MHz
- operating frequency range (max.) set by a resistor, and (min.) by a capacitor and resistor.
- pulse width set by a resistor and capacitor
- low start-up current
- overload shutdown with delayed soft restart
- overvoltage/undervoltage shutdown
- soft-start
- single-ended output
- drives power MOSFETs directly (1.6 A peak)
- low cost 16 pin DIP or SOIC

ABSOLUTE MAXIMUM RATINGS

Parameter	Value & Units
Supply Voltage	20 V
Undervoltage/Overvoltage Input	-0.4 V - 6 V
Overload Input	-0.4 V - 6 V
Remote Shutdown	-0.4 V - V_{CC}
VCO Input	-0.4 V - V_{CC}
Storage Temperature	-65°C ≤ T_S ≤ 150°C
Lead Temperature (soldering, 10 sec.)	260°C
Junction Temperature	150°C
Power dissipation at T_A ≤ 70°C (derate 9 mW /°C for T_A > 70°C)	720 mW



PIN CONNECTION
16 PIN DIP

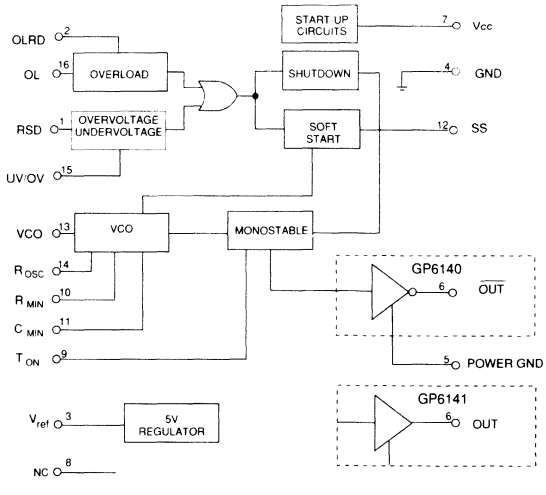
CIRCUIT DESCRIPTION

The features of the GP6140 and GP6141 are specifically designed to support the Zero Voltage Switching (ZVS) topologies. The controllers support resonant and quasi-resonant circuits operating in variable frequency, fixed pulse mode. The pulse is held constant while the frequency is varied by the voltage on the VCO input. The maximum frequency is set by an external resistor, and the minimum is determined by a capacitor and resistor combination. The fixed pulse width is set by a resistor and capacitor network.

The controllers feature such peripheral functions as soft-start from the maximum frequency, undervoltage/overvoltage shutdown with delayed restart. The power supply undervoltage lockout minimizes supply current during the start-up condition.

The Zero Voltage Switching operation results in an even higher reduction of switching losses in the power transistor. Due to the high frequency operation a cost reduction of the main power components can be achieved.

FUNCTIONAL BLOCK DIAGRAM



Document No. 510 - 97-1

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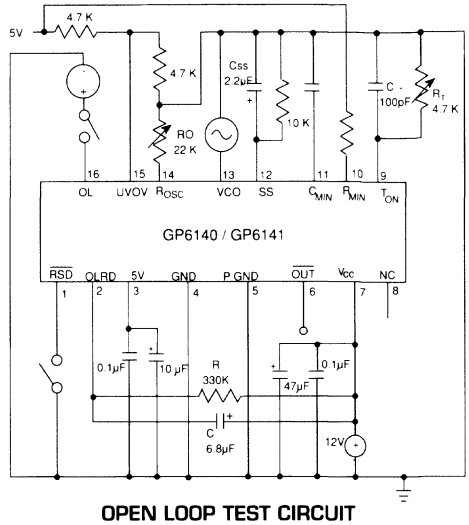
Part Number (10 digits)	Package Type	Temperature Range
GP6140-CDC GP6141-CDC	16 Pin DIP	0° to 70° C
GP6140-CKC GP6141-CKC	16 Pin SOIC	0° to 70° C
GP6140-EDC GP6141-EDC	16 Pin DIP	-40° to 85° C
GP6140-EKC GP6141-EKC	16 Pin SOIC	-40° to 85° C
GP6140-MDC GP6141-MDC	16 Pin DIP	-55° to 125° C

ORDERING INFORMATION



OPEN LOOP TEST CIRCUIT

ELECTRICAL CHARACTERISTICS

Limits apply over
$0°C \le T_A \le 70°C$ for the GP6140/41CDC, andGP6140/41CKC
$-40°C \le T_A \le 85°C$ for the GP6140/41EDC, and GP6140/41EKC
$-55°C \le T_A \le 125°C$ for the GP6140/41MDC

Parameters tested on open loop test circuit
Typical values are at $I_A = 25°C$
★ Parameters marked with an asterisk* are valid only at $T_A = 25°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Chip Supply					
Supply Voltage		10	12	20	V
Chip Enable V_{CC} Threshold *		-	13.0	-	V
V_{CC} Undervoltage Lockout *		-	9.0	-	V
Supply Current	V_{CC} = 11 V (UV condition) V_{CC} = 12 V	- 18	2 24	5 26	mA mA
Voltage Control Oscillator					
Maximum Frequency		2.4	3	-	MHz
Tolerance of f_{MAX} * Tolerance of f_{MIN} *	C_O = 100 pF V_{VCO} = 10 V R_O = 12 kΩ V_{VCO} = 0 V	- -	- -	±5 ±5	% %
Temperature coefficient f_{MAX} Temperature coefficient f_{MIN}	R_O = 12 kΩ C_O = 100 pF R_T = 4.7 kΩ C_T = 100 pF	-400 -400	-700 0	-900 400	ppm/°C ppm/°C
Dead Time T_{OFF} *		-	90	-	ns
Operating Range of VCO Input (Pin 13)	max min	- -	8 3	- -	V V
Internal Pull-up Resistor (Pin 13) *		9.6	12	14.4	kΩ
Output Pulse Width T_{ON} Tolerance *	R_T = 4.7 kΩ C_T = 100 pF	-	-	±5	%
Temperature Coefficient of T_{ON}	T_{ON} = 500 ns GP6040	-	-200	-	ppm/°C
	GP6041	-	-780	-	ppm/°C

ELECTRICAL CHARACTERISTICS continued

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Section					
Output Risetime	100 pF II 100 kΩ load on $\overline{OUT}$	-	10	30	ns
Output Falltime	(See Fig. 7)	-	10	30	ns
Output Low Level (sink) *	I_{OUT} = 20 mA	-	-	0.7	V
	I_{OUT} = 200 mA	-	-	2.2	V
Output High Level (source) *	I_{OUT} = -20 mA	V_{CC} -2.0	-	-	V
	I_{OUT} = -200 mA	V_{CC} -2.2	-	-	V
Reference Section					
Output Voltage *	I_{REF} = 10 mA	4.75	5.00	5.25	V
Temperature Stability		-200	100	300	ppm/°C
Maximum Current Capability		-	10	-	mA
Shutdown Section					
Prop. Delay to Shutdown		-	300	400	ns
Overload Shutdown (OL) Threshold *		3.04	3.2	3.36	V
OL Threshold Temp. Coefficient		-400	100	500	ppm/°C
OL Hysteresis		-	3	-	%
OL Trigger Pulse Width		500	-	-	ns
OL Input Current Range (Pin 14)		-1	-	+15	µA
Overvoltage Threshold Lockout *		3.04	3.2	3.36	V
Undervoltage Threshold Lockout *		-	1.9	2.0	V
Temp. Coeff. of Threshold Voltage		-400	100	500	ppm/°C
Hysteresis of the Lockout Voltage		-	4	-	%
Input Current Range (Pin 13)		-1	-	+22	µA
Thermal Impedance	16 pin DIL Plastic Pack. θ JC	-	42	-	°C/W
	16 pin DIL Plastic Pack. θ CA	-	70	-	°C/W
	16 Pin SOIC θ JA	-	112	-	°C/W

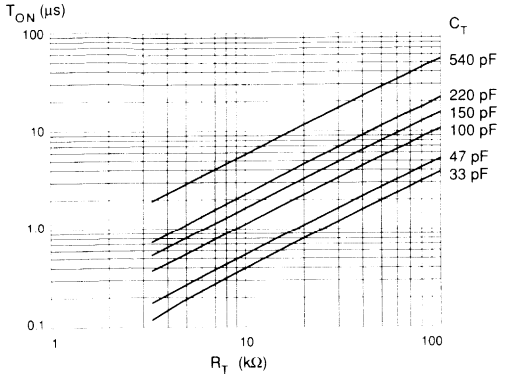


Fig. 1 Output Pulse Width GP6140

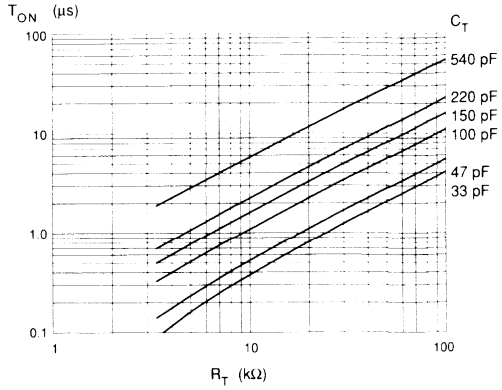


Fig. 2 Output Pulse Width GP6141

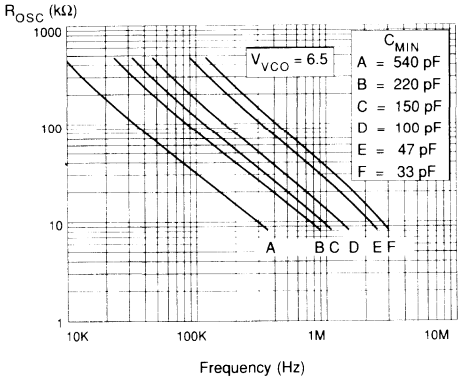


Fig. 3 Maximum Operating Frequency GP6140/41

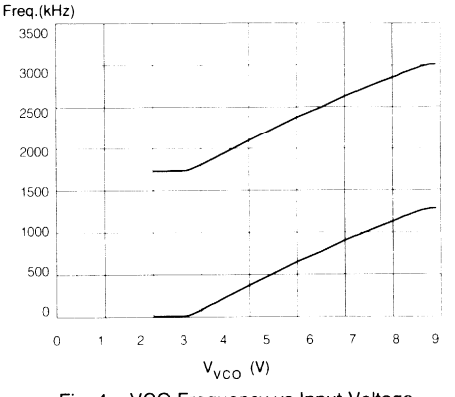


Fig. 4 VCO Frequency vs Input Voltage GP6140 / 41

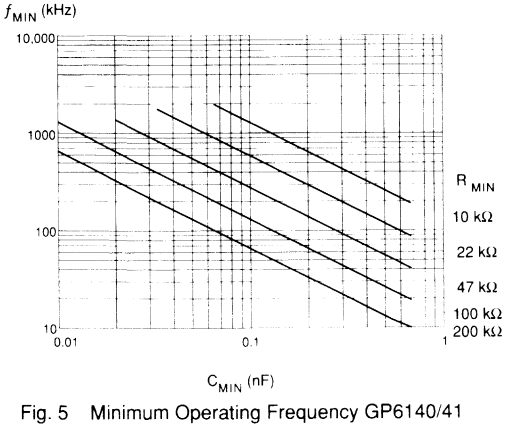


Fig. 5 Minimum Operating Frequency GP6140/41

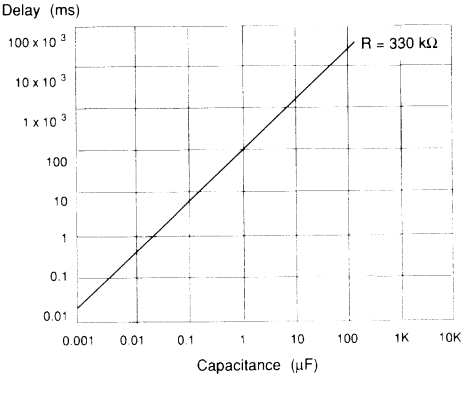


Fig. 6 Overload Restart Delay GP6140/41

TYPICAL PERFORMANCE CURVES OF THE GP6140 AND GP6141

For all graphs, V_{CC} = +12 volts DC and T_A = 25 °C. The curves shown above represent typical batch sampled results.

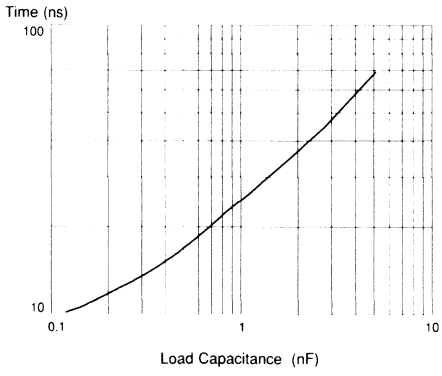


Fig. 7 Output Risetime/Falltime GP6140/41

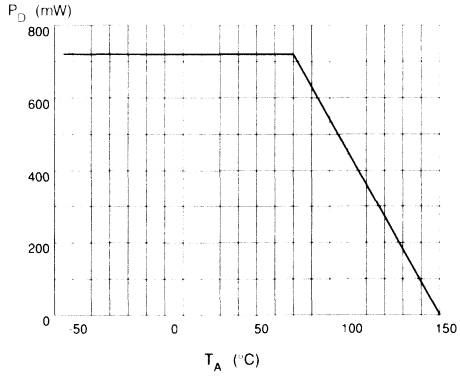


Fig. 8 Power Dissipation GP6140/41

PIN FUNCTIONS

Pin 1 (RSD) - Remote Shutdown

A low level (or in current mode - high sink current) on Pin1 shuts down the GP6140 or GP6141. When the pin is released (in current mode - zero current), the controller goes to soft-start. If remote shutdown is not used, leave Pin 1 open. In Fig. 9 the simplified remote shut-down internal circuit is shown.

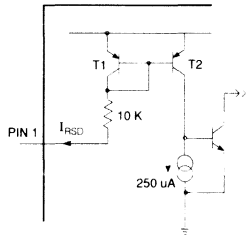


Fig. 9

The transistors T1 and T2 constitute the current mirror. To activate shutdown it is necessary to source from the GP6140 or GP6141 current I_{RSD} = 250 µA (min). The ability to choose between current or voltage mode shutdown allows for operation in a noisy environment.

Pin 2 (OLRD) - Overload Restart Delay

This input sets the overload restart delay if pin 16 (Overload sense) is activated. Timing starts when the overload is removed; upon time-out, soft-start begins. Refer to Fig. 6 to select proper value of the capacitor. Recommended value of the bias resistor is 330 kΩ. For overload restart delay time, it makes no difference if the capacitor is connected to the ground or to the V_{CC} line. However if the capacitor is connected to the ground, during initial power-up condition, the soft-start will be delayed by the time equal to the overload restart delay time. If the capacitor is connected to the V_{CC} line, soft-start follows an internal delay time of 1ms (necessary to stabilize +5 V reference line).

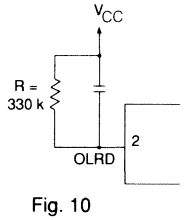


Fig. 10

Pin 3 (V_{REF}) - +5V Reference

The 5% tolerance regulator is used to power most of the internal circuitry. It can be used as a reference for external circuitry as long as the load is less than 10 mA. For a 1% tolerance regulator contact Gennum's Power Products Department.

To improve noise rejection ratio it is recommended to decouple pin 3 to the logic ground with a 2.2 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor.

Pin 4 (GND) - Ground

Great care must be taken to ensure that grounds are run so that any voltage drops from high ground currents are minimized and do not interfere with feedback voltages and references.

Pin 5 (PGND) - Power Ground

Only the output transistor should be connected to the power ground, to minimize interference with the logic circuitry. GND and PGND are to be connected outside the package. The connection point should be carefully chosen and decoupled.

Pin 6 (OUT) - Output

The GP6140 provides an active low fixed pulse width output and low level in the standby condition. The GP6141 provides an active high fixed pulse width output and high level in the standby condition. For the risetime and falltime characteristics refer to Fig.7.

Pin 7 (V_{CC}) - Supply Voltage

The power supply trace must be decoupled as close to pin 7 as possible. Currents of 1.6 A levels may be drawn by the GP6140 and GP6141. Minimum recommended decoupling is a 10 µF tantalum capacitor in parallel with 0.1 µF ceramic capacitor.

The controller is equipped with a low start-up current circuit. The hysteresis is adjusted as follows: turn on at 13 V (typ) and turn off if the voltage drops to 9 V (typ).

Pin 8 (NC) - Not Connected

Pin 9 (T_{ON}) - Pulse Width

The constant pulse width T_{ON} is set by a resistor R_T and capacitor C_T. This relationship is shown in Fig.1 for GP6140 and Fig. 2 for GP6141. $R_T \times C_T$ should have a temperature coefficient of +200 ppm/°C (GP6140) and +750 ppm/°C (GP6141) for best stability. The T_{ON} time is generated by a monostable multivibrator and may have any required duration. The only limit is the minimum value of the resistor $R_T \geq 3.3\ k\Omega$ due to the current capability of the pin 9. The monostable works in re-triggerable mode. It means that if the maximum frequency set by external components is higher than specified in description of the pin 14, the T_{ON} time remains constant, however the frequency will divide by two. This feature could be used as an inherent current limit. Under normal operation f_{MAX} should be clamped by proper choice of the resistor R_{OSC}.

Pin 10 (R_{MIN}) - F_{MIN} Oscillator Resistor

The resistor on this pin, R_{MIN}, together with the oscillator capacitor, C_{MIN}, on pin 11 controls the minimum frequency (f_{MIN}) of the VCO operating range. The resistor R_{MIN} and capacitor C_{MIN}, must be selected as the first components of the oscillator section. Refer to Fig. 5 for selection.

Pin 11 (C_{MIN}) - f_{MIN} Oscillator Capacitor

The capacitor on this pin, C_{MIN} together with oscillator resistor on pin 10, R_{MIN}, controls the minimum frequency (f_{MIN}) of the VCO operating range. The capacitor, C_{MIN}, and resistor R_{MIN} must be selected as the first components of the oscillator section. Refer to Fig. 5 for selection.

Pin 12 (SS) - Soft-Start

A capacitor C_{SS} on this pin provides a controlled start-up from f_{MAX} to the frequency set by the VCO input. The value of the C_{SS} is not limited. To ensure a full soft-start after UVOV fault, it is necessary to have the fault present for half the soft-start time (to ensure discharge of the C_{SS} capacitor).

Pin 13 (VCO) - Voltage Controlled Oscillator Input

The VCO input is designed for an optocoupler feedback network from the secondary (output) side of the power supply. An internal 12 kΩ (typ.) pull-up resistor is provided but an external resistor may be used if a lower value is required. The control characteristic is shown in Fig. 4 .

Pin 14 (R_{OSC}) - Oscillator Resistor

The resistor on this pin, R_O, controls f_{MAX} : the maximum frequency of the VCO operating range. Refer to Fig. 3 for selection of R_O. This resistor should be selected after C_{MIN} and R_{MIN} is chosen. The use of a 1%, zero temperature coefficient resistor is recommended for good stability. Minimum value for R_{MIN} is 8.2 kΩ. For normal operation the maximum frequency should be set no higher than:

$$f_{MAX} \leq \frac{1}{T_{ON} + T_{DT}}$$

where T_{ON} - constant pulse width

T_{DT} - dead time specified in the data sheet.

If this requirement is not fulfilled the controller divides the output frequency by two.

Pin 15 (UVOV) - Undervoltage/Overvoltage Shutdown

This input is a window comparator. A higher or lower voltage than the thresholds specified will shutdown the power supply until the input voltage falls within the window again, at which point the GP6140 or GP6141 goes into soft-start. If Pin 15 is not used, it must be tied to V_{CC} via a voltage divider generating a bias voltage which falls within the window. The maximum input voltage on this pin is 6 V. To adjust the shutdown hysteresis levels use an additional resistor connected to the +5 V line.The value of the resistors can be calculated from the equations:

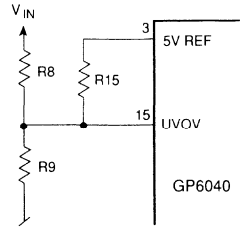


Fig. 11

$$R15 = \frac{(V_O \times V_R) - (V_U \times V_R)}{(V_U \times V_{INO}) - (V_O \times V_{INU})} \times R8$$

$$R9 = \frac{R8 \times V_R \times (V_O - V_U)}{V_R \times (V_{INO} - V_{INU} + V_U - V_O) + (V_O \times V_{INU} - V_U \times V_{INO})}$$

where V_O - the GP6140/41 overvoltage threshold lockout
V_U - the GP6140/41 undervoltage threshold lockout
V_R - reference voltage
V_{INO} - requested line overvoltage lockout
V_{INU} - requested line undervoltage lockout

Pin 16 (OL) - Overload Input

A voltage exceeding the specified threshold on this pin will cause the GP6140 or GP6141 to synchronously shutdown and activate the overload restart delay function. This delay starts when the input voltage drops below the threshold. On time-out Soft-start begins. The maximum input voltage on this pin is 6 V. If pin 16 is not used, short it to ground.

AVAILABLE PACKAGING

16pin DIP	16 pin SOIC

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REVISION DATE Apr 1990

GENNUM CORPORATION

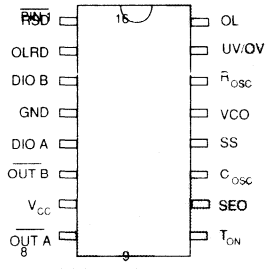
Resonant Mode Power Supply Controller

LD405 DATA SHEET

FEATURES

- **frequency range of 10 kHz to 1 MHz**
- **operating frequency range (min. and max.) set by a resistor and capacitor**
- **pulse width set by a resistor and a capacitor**
- **synchronous overload shutdown with restart delay**
- **synchronous overvoltage, undervoltage and remote shutdown**
- **soft-start**
- **single-ended or complementary outputs**
- **drives power MOSFETs directly**
- **low cost 16 pin DIP or SOIC**

TOP VIEW



PIN CONNECTION
16 PIN DIP

CIRCUIT DESCRIPTION

The LD405 utilizes frequency modulation instead of pulse width modulation to achieve regulation. The pulse width is held constant while the frequency is varied over an operating range set by a resistor and capacitor. A feedback voltage controls the switching frequency of the two complementary outputs, which are capable of driving power MOSFETs directly.

Opening a normally grounded control pin puts the LD405 into single-ended operation. In this mode the frequency is doubled and the two outputs are identical so they can be paralleled for increased drive capability. The high operating frequency of up to 1 MHz results in significant reductions in the size of the required magnetic and capacitive components. This leads to dramatic savings in volume, weight and manufacturing cost of switching power supplies.

Included on the chip are peripheral functions such as soft-start, undervoltage/overvoltage lockout, remote shutdown and overload shutdown with delayed restart. All shutdown modes are synchronous (the last output pulse is completed), and default to soft-start once the fault condition is removed.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range
LD405D	16 Pin DIP	0° to 70° C
LD405K	16 Pin SOIC	0° to 70° C

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Document No. 510 - 4 - 2

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Tokyo Office: 301 Aoba Building, 3-6-2, Minato-ku, Tokyo 108, Japan tel. (03) 441-2096 fax: (03) 448-8991

GENNUM CORPORATION

Current Mode PWM Controller

GP2842 DATA SHEET

FEATURES

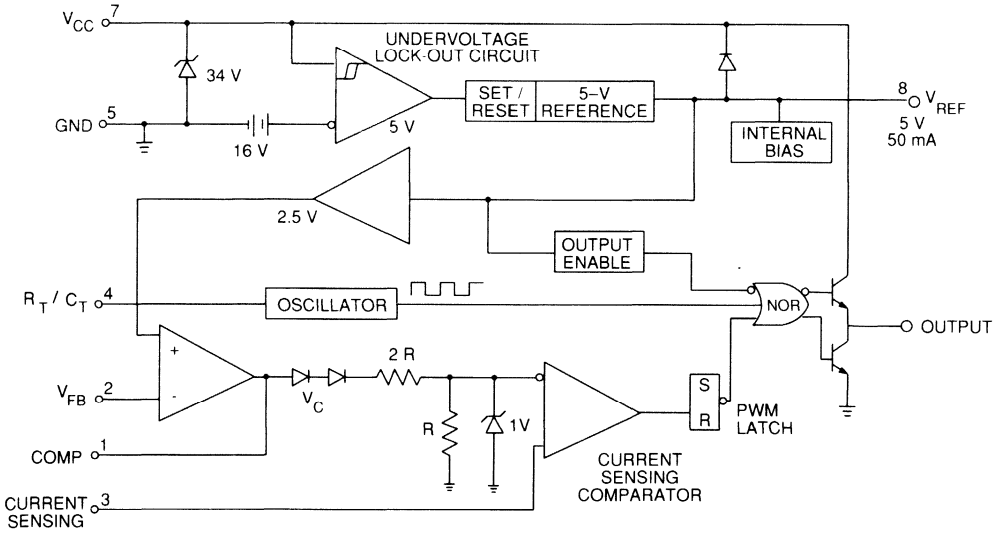
- optimized for off-line control
- internally trimmed temperature compensated oscillator
- maximum duty-cycle clamp
- V_{REF} stabilized before output stage is enabled
- low startup current
- pulse-by pulse current limiting
- improved U/V lockout
- double pulse suppression
- 1% trimmed bandgap reference
- high current totem pole output

CIRCUIT DESCRIPTION

The GP2842 series of current-mode control ICs are available in an 8 pin mini-dip package. They provide all the features necessary to implement off-line, fixed frequency current-mode control with a minimum of external components.

GP2842 incorporates a new precision temperature controlled oscillator with an internally trimmed discharge current to minimize variations in frequency. A precision duty-cycle clam eliminates any need for an external oscillator when at, or near, a 50% duty-cycle condition. Duty-cycle greater than 50% are also possible. Special logic ensures that V_{REF} is stablized before the output stage is enable. I_{ON}-implant resistor provide tighter control of under-voltage lockout.

Other features include low startup current, pulse-by-pulse current limiting, and a high-current totem pole output for driving capacitive loads, such as the gate of a power MOSFET. The output is low in the off state, consistent with N-channel devices.



Block Diagram

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ABSOLUTE MAXIMUM RATINGS

Parameter	Value / Units
Supply Voltage (I_{CC} < 30 mA	Self Limiting
Supply Voltage (Low Impedence Source)	30 V
Output Current	± 1 A
Output Energy (Capacitive Load)	5 µ J
Analog Inputs (Pin 2, Pin 3)	- 0.3 V to V
Error Amp Output Sink Current	10 mA

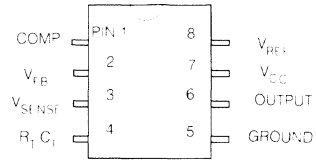

Fig. 1 Pin Connection

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, specifications apply for -25 ≤ T_A ≤ 85 C V_{CC} = 15 V (Note 1), R_T = 680 Ω, C_T = .022 µF

Parameter	Conditions	Min.	Typ.	Max.	Units
Reference Section					
Output Voltage	T_J = 25°C, I_O = 1 mA	4.95	5.00	5.05	V
Line Regulation	12 ≤ V_{IN} ≤ 25 V	-	6	20	mV
Load Regulation	1 ≤ I_O ≤ 20 mA	-	6	20	mV
Temp. Stability	(Note 2)	-	0.2	0.4	mV / °C
Total Output Variation	Line, Load, Temp. (Note 2)	4.90	-	5.10	V
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, T_J = 25°C (Note 2)	-	50	-	µV
Long Term Stability	T_A = 125°C, 1000 hours (Note 2)	-	5	25	mV
Output Short Circuit	T_A = 25°C	-30	-100	-180	mA
Oscillator Section					
Initial Accuracy	T_J = 25°C	47	52	57	kHz
Voltage Stability	12 ≤ V_{CC} ≤ 25 V	-	0.2	1	%
Temp. Stability	T_{MIN} ≤ T_A ≤ T_{MAX} (Note 2)	-	5	-	%
Amplitude	$V_{PIN\ 4}$ peak to peak	-	1.7	-	V
Discharge Current	T_J = 25°C T_{MIN} ≤ T_A ≤ T_{MAX}	7.8 7.5	8.3 -	8.8 9.0	mA mA
Error Amp Section					
Input Voltage	$V_{PIN\ 1}$ = 2.5 V	2.45	2.50	2.55	V
Input Bias Current		-	-0.3	-1	µA
A_{VOL}	2 ≤ V_O ≤ 4 V	65	90	-	dB
Unity Gain Bandwidth	(Note 2)	0.7	1	-	MHz
PSRR	12 ≤ V_{CC} ≤ 25 V	60	70	-	dB
Output Sink Current	$V_{PIN\ 2}$ = 2.7 V, $V_{PIN\ 1}$ = 1.1 V	2	6	-	mA
Long Source Current	$V_{PIN\ 2}$ = 2.3 V, $V_{PIN\ 1}$ = 5 V	-0.5	-0.8	-	mA
V_{OUT} High	$V_{PIN\ 2}$ = 2.3 V, R_L = 15 kΩ to ground	5	6	-	V
V_{OUT} Low	$V_{PIN\ 2}$ = 2.7 V, R_L = 15 kΩ to Pin 8	-	0.7	1.1	V

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated, specifications apply for $-25 \le T_A \le 85°C$ V_{CC} = 15 V (Note 1). R_T = 680 Ω. C_T = .022 µF

Parameter	Conditions	Min.	Typ.	Max.	Units
Current Sense Section					
Gain	(Note 3 & 4)	2.85	3	3.15	V / V
Maximum Input Signal	$V_{PIN\ 1}$ = 5 V (Note 3)	0.9	1	1.1	V
PSRR	$12 \le V_{CC} \le 25$ V (Note 3)	-	70	-	dB
Input Bias Current		-	-2	-10	µA
Delay to Output	T_J = 25°C (Note 2)	-	150	300	ns
Output Section					
Output Low Level	I_{SINK} = 20 mA	-	0.1	0.4	V
	I_{SINK} = 200 mA	-	1.5	2.2	V
Output High Level	I_{SOURCE} = 20 mA	13	13.5	-	V
	I_{SOURCE} = 200 mA	12	13.5	-	V
Rise Time	T_J = 25°C, C_L = 1 nF (Note 2)	-	50	150	ns
Fall Time	T_J = 25°C, C_L = 1 nF (Note 2)	-	50	150	ns
Output Leakage	V_{CC} = 14 V, UVLO Active, $V_{PIN\ 6}$ = 0	-	-0.01	-10	µA
Total Standby Current					
Startup Current		-	0.5	1	mA
Operating Supply Current	$V_{PIN\ 2} = V_{PIN\ 3}$ = 0V, R_T = 10 kΩ, C_T = 3.3 nF	-	11	17	mA
V_{CC} Zener Voltage	I_{CC} = 25 mA	-	34	-	V
Undervoltage Lockout Section					
Start Threshold		15	16	17	V
Minimum Operating Voltage	After Turn ON	9	10	11	V

Notes: 1. Adjust V_{CC} above the start threshold before setting at 15 V.

2. These parameters, although guaranteed, are not 100% tested in production.

3. Parameter measured at trip point of latch with $V_{PIN\ 2}$ = 0.

4. Gain defined as: $A = \frac{\Delta V_{PIN\ 1}}{\Delta V_{PIN\ 3}}$, $0 \le V_{PIN\ 3} < 0.8$ V.

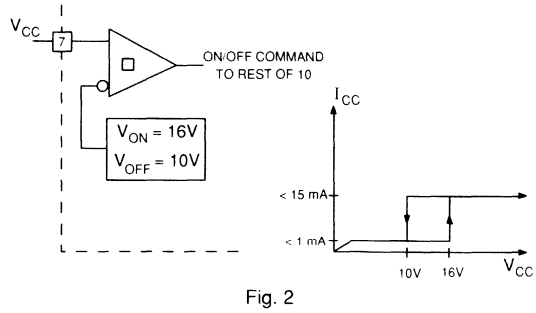

Fig. 2

During undervoltage lock-out, the output driver is biased to a high impedance state. Pin 6 should be shunted to ground with a bleeder resistor to prevent output leakage current from activating the power switch.

ORDERING INFORMATION

Part Number (10 digits)	Package Type	Temperature Range
GP2842 ID	16 Pin DIP	-25° to 85° C

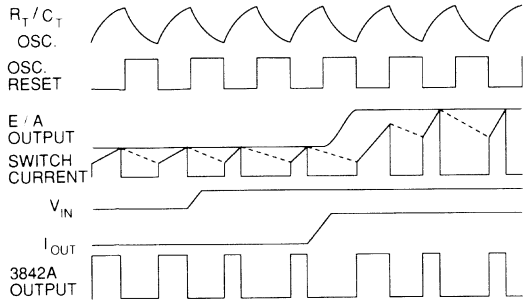

Fig. 3 Timing Diagram

GP2842 Timing

To generate the PWM waveform the control voltage from the error amplifier is compared to a current sense signal which represents the peak output inductor current. An increase in V_{IN} causes the inductor current slope to increase, thus reduicing the duty cycle. This is an inherent feed-forward characteristic of current mode control, since the control voltage does not have to change during changes of input supply voltage.

When the power supply sees a sudden large output current increase, the control voltage will increase allowing the duty cycle to momentarily increase. Since the duty cycle tends to exeed the maximum allowed, to prevent transformer saturation in some power supplies, the internal oscillator wave form provides the maximum duty cycle clamp as programmed by the selection R_T/C_T components.

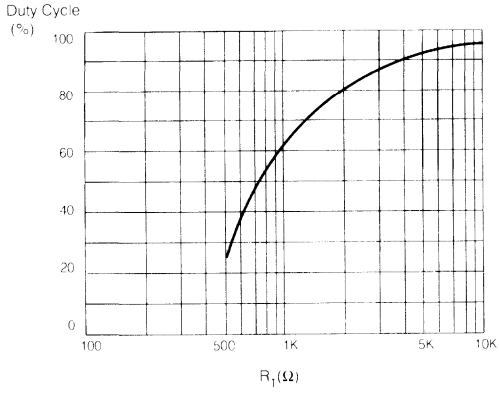

Fig. 4 Oscillator Duty Cycle vs R_T

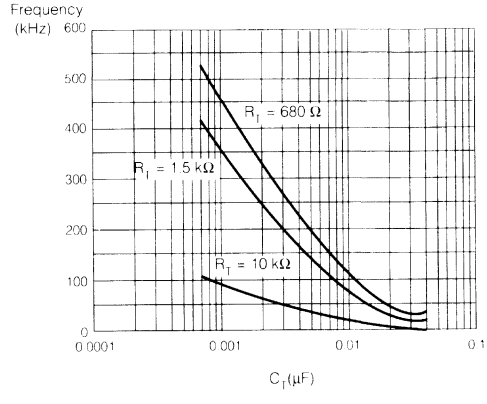

Fig. 5 Oscillator Frequency vs C_T

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The GP605 in a Variable Frequency Zero Current Switching, Half Bridge Resonant Mode Power Supply

APPLICATION NOTE

1.0 INTRODUCTION

The continuous trend towards reducing the size of power converters forces designers to increase operating frequencies. Conventional quasi-square pulse converters are now approaching the 300 to 500 kHz range. This allows about a 3:1 reduction in the size of the major passive components, such as magnetics and capacitors, as compared to 20 kHz switchers. But these converters (mostly pulse width controlled converters), obviously have higher switching losses in power semiconductors (see Figure 1a), despite the use of MOSFETs. The resulting inefficiency requires larger heatsinks, and thus defeats the goal of reducing the size.

There is, however, a more efficient way to convert power at ever higher frequencies. It is called ***zero current switching or sinewave current switching*** (see Figure 1b). Such a waveform can be generated by either a parallel or series resonating LC tank. The resulting class of converters is called ***resonant***.

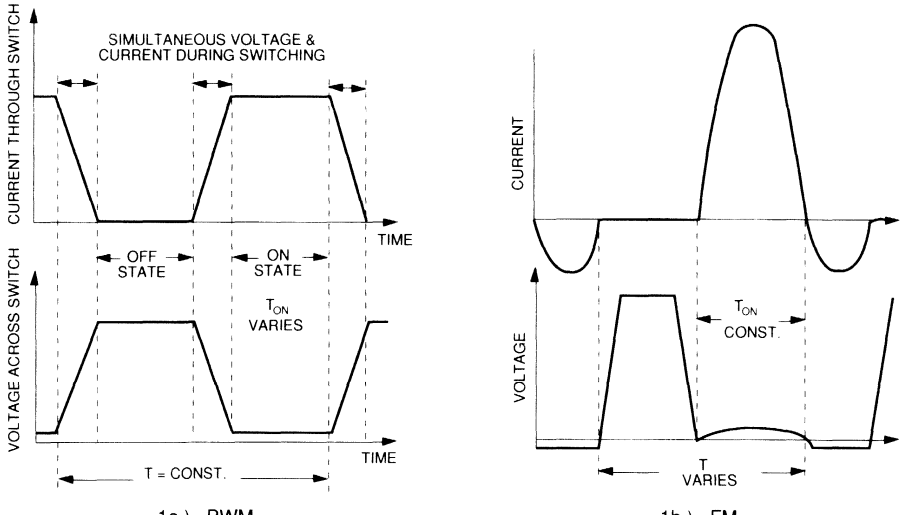
The clear advantage of sinewave current is that, as switching generally occurs at zero current, switching losses in power semiconductors are almost eliminated. The primary disadvantage of a resonant converter is that for a given power level, the actual peak current is 3 to 4 times greater than that of a PWM converter. This can be overcome by using lower on resistance semiconductors, creating a practical means to increase operating frequencies up to 1 MHz and higher. These frequencies allow designers to achieve power densities in excess of 25 watts/cubic inch, which is about 4 times better than is possible at 100 kHz.

There are many types of resonant and quasi-resonant topologies. Besides a sinewave switching current, most of them employ FM control, which provides a fixed on time (T_{ON}), and variable period T. Conversely, PWM uses fixed period, variable on time.

This application note describes a 125W resonant mode power supply, with Gennum's GP605 performing both control and housekeeping functions.

The GP605 is an upgraded version of the first commercially available resonant mode controller - Gennum's LD405. This IC combines all the necessary features of modern power controllers.

If you are not familiar with the GP605 please refer to Gennum's data sheet 510-43.



1a) PWM 1b) FM

Fig. 1 GP605 Block Diagram

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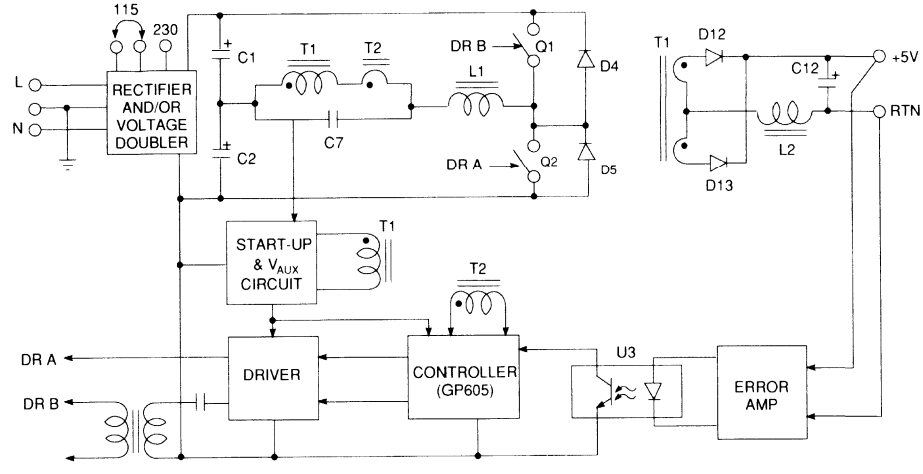


Fig. 2 Block Diagram of an Off-line Unit (115V AC or 230V AC)

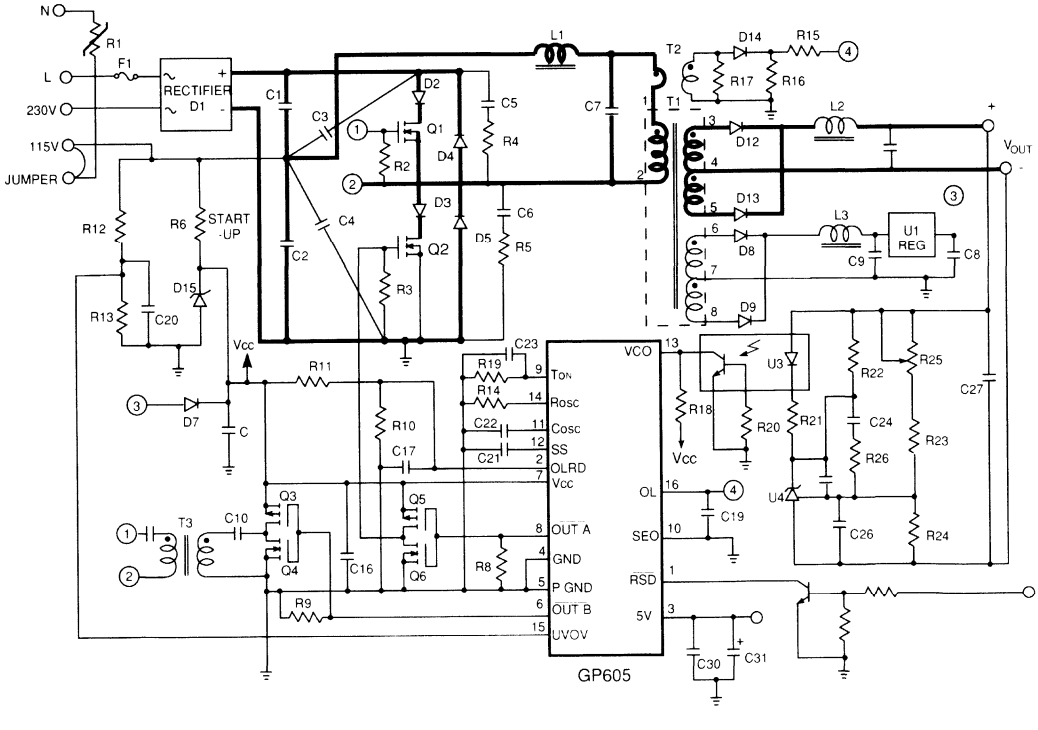


Fig. 3 Detailed Schematic of the Supply for Figure. 2

2.0 RESONANT POWER SUPPLY

A Rectifier/Voltage Doubler block provides an unregulated 300V DC (VNR) bus for the high frequency resonant converter. A resonating tank, consisting of an inductor L1 and capacitor C7, is connected in series. Sinusoidal voltage across the capacitor C7 to the output stage is stepped down via the power transformer T1. As far as the driving sequence is concerned, this resonant converter operates similarly to a half bridge square pulse converter. During the first resonating cycle switch Q2 is off. The full cycle takes place in Q1, the parallel combination of C7 and the primary winding on T1 (along with one turn of the current sense transformer T2), and inductor L1. The return current flows via diode D4. Capacitor C1 serves as a voltage source for this cycle.

In the second resonating cycle switch Q2 is on and Q1 is off. The second cycle takes place in Q2, the inductor L1, and the parallel combination of C7, and the primary winding on T1 (again one turn on the current sense transformer T2). The return current in this case flows via diode D5. Note that the current in the second cycle has reversed its polarity as compared to the current in the first cycle, thus transformer T1 works in a bipolar mode. Capacitor C2 serves as a voltage source for the second cycle. During the period of time when switch Q2 is off, diode D4 clamps the voltage across Q2 to the level of the VNR bus. The diode D5 does the same thing for switch Q1. Thus switches Q1 and Q2, as well as diodes D4 and D5, can be rated to only 420 volts. Therefore the high line (132 VAC RMS or 264 VAC RMS) after being doubled and rectified, still leaves a safety margin of about 50 volts.

The output stage is fairly straightforward. It is a full-wave Schottky, centre-tap rectifier, composed of D12, D13, L2, and output capacitor C12. The output here is 5 VDC at 25 amps.

Regulation is achieved by changing the commutating frequency of the controller GP605. Its VCO gets the input signal from an error amplifier via the optical coupler U3. The controller also performs the following functions:

- soft-start
- hiccup current limit
- VNR bus undervoltage and overvoltage shutdown
- remote shutdown

In order to provide fast turn-on and turn-off of the power switches Q1 and Q2, driving requires an additional stage. Although the average power needed to drive both switches is under 1 watt, it takes up to 0.75A of short-duration current pulses to charge and discharge the gate source capacitance of the MOSFET switches Q1 and Q2. This is achieved by using totem-pole type MOSFET stages. Transistors Q5 and Q6 drive switch Q2, while transistors Q3 and Q4 drive switch Q1 via a pulse transformer T3.

The controller and driver are powered by the 12V DC V_{AUX} bus. During start-up this voltage is supplied from one half of the VNR bus via thermistor R6, and zener diode D15.

About 18V is supplied to the V_{AUX} bus on start-up. Once the supply is up and running (about 20 ms) V_{AUX} is supplied by the additional winding, 6-8, of the power transformer T1. The voltage from this winding is rectified and regulated to the level of 12 V ±5%.

The supply utilizes primary current sensing. This involves the primary winding of the power transformer T1 being connected in series with a single turn winding of the $^1/_4$ inch diameter current-sensing transformer T2. This transformer has a turns ratio of 1:40. Its secondary winding voltage is in linear proportion to the primary winding current, and the voltage pulses look like current pulses in the primary of the power transformer T1.

After rectification and some filtering, an essentially sawtooth voltage level, (which is proportional to the total load), is applied to pin 16 of the controller. Once this sawtooth reaches a programmed threshold, the controller shuts down for approximately 1 second. This waiting period is set by a 4.7 µF tantalum capacitor connected to pin 2. When it has elapsed, the controller starts generating its pulse-train. Initially the pulse frequency is approximately 10 kHz, then increases, following a preset time constant. In about 20 ms the power supply either reaches a normal regulation mode, or if the overload condition on the output continues, it goes into shutdown again. The supply will stay in the hiccup mode until the overload is removed.

The maximum commutating frequency of this supply is 600 kHz (300 kHz per transistor) and the resonating frequency of the C7-L1 tank is about 750 kHz.

The value of C7 is 8200 pF and the value of L1 is 5 µH. The resonating frequency f_R can be calculated from the following equation:

$$f_R = \frac{1}{2\pi\sqrt{C_R L_R}}$$

where C_R and L_R are resonating components.

The primary power transformer winding inductance is at least 100 times higher than that of L1, therefore it does not affect the resonating frequency f_R.

3.0 DESIGN SEQUENCE

3.1 Integrating the GP605 into the Power Supply

3.1.1 Maximum VCO Frequency

In this design f_{MAX} is set at 600 kHz. For the oscillator capacitor (C_{OSC}), a temperature stable NPO (COG), ceramic, 150 pF capacitor is recommended. Keep the leads on this capacitor very short to minimize the parasitic inductance. According to Gennum's data sheet 510-43, R_{OSC} - 17.4 kΩ, 1%. Tolerance of f_{MAX} from chip to chip is ±5% (570 kHz to 630 kHz).

3.1.2 Set Output Pulse Width (T_{ON})

The timing for the MOSFET switch Q1 (Q2) is set to shut off during the diode D4 (D5) conduction, (see Figure 1). The best method of doing this is to terminate the T_{ON} pulse right in the middle of a negative half of a sine wave current:

$$T_{ON} = 0.75 \frac{1}{f_R}$$

Then relative inaccuracy in T_{ON} will not affect the circuit 's operation. In this case f_R =750 kHz, and T_{ON} = 1 µs. A 100pF capacitor is chosen and placed in series with R_T (R19) whose value is determined to be 9.4 kΩ, as seen from the graph (Figure 2) in data sheet 510-43.

3.1.3 Soft-start Capacitor

Capacitor C21 is needed to provide a relatively slow change in the VCO operating frequency , from minimum value (about 11 kHz for C_{OSC} = 150 pF) to the value which is set by the feedback loop. The result is a soft start-up of the power supply. Usually 2 to 3 cycles of the input AC line are sufficient to charge the input filter capacitors. This means that 30 ms to 48 ms Soft-start Delay (50-60 Hz) is necessary. A 4.7 µF capacitor value provides about 40 ms of soft-start (see 510-43 data sheet pin description). The higher the power level of the converter, the longer the soft-start time is needed. A value of 100 to 200 ms could be used for a 500 W supply.

3.1.4 VCO Input

In this application design, the input voltage is set by an error amplifier via an optocoupler. The proper level of the current in the photo-transistor is set by an external resistor R18. If the VCO input is set at 4.0 V, (in the middle of the 1.5 V - 6.5 V range of VCO), and V_{CC} = 12 V, the parallel combination of 10 kΩ internal pull-up resistor and external R18 resistor, is about 2.3 kΩ. Thus R18 = 3 kΩ.

3.1.5 UVOV Shutdown

This pin is used to set the input voltage operating range for the power supply. The nominal value for the rectified 220 V AC bus is about 350 V (taking input diode drops into consideration). Normally this pin level is set to 2.5 volts.

Resistive divider R12 - R13 carries just under 1 mA of current. Having R12 = 360 kΩ and R 13 = 3 kΩ sets up the range from 220 V DC (78 V AC x 2 x 1.4) to 390 V DC (138 V AC x 2 x 1.4) which is quite acceptable for most designs. To change undervoltage and overvoltage threshold levels, apply resistance between UVOV input (pin 15) and reference voltage (pin 3)(Fig. 4).

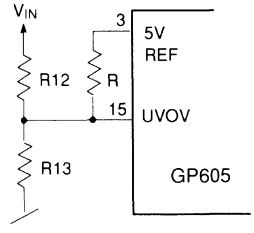


Figure 4

The value of the resistors can be calculated from the equations:

$$R = \frac{(V_O \times V_R) - (V_U \times V_R)}{(V_U \times V_{INO}) - (V_O \times V_{INU})} \times R12$$

$$R13 = \frac{R12 \times V_R \times (V_O - V_U)}{V_R \times (V_{INO} - V_{INU} + V_U - V_O) + (V_O \times V_{INU} - V_U - V_{INO})}$$

where V_O - the GP605 overvoltage threshold lockout
V_U - the GP605 undervoltage threshold lockout
V_R - reference voltage
V_{INO} - requested line overvoltage lockout
V_{INU} - requested line undervoltage lockout

3.1.6 Overload Protection (OL)

The current sensing is provided by the current transformer T2. With a turns ratio of 1 : 40 it reduces the primary current of the power transformer T1, by a factor of 40. Only positive pulses pass by diode D14. The resulting voltage drop across resistor R16, is applied to pin 16 (OL) of the GP605 via resistor capacitor filter R15 - C19. The time constant of this filter is 3.5 µs. Therefore the voltage across C19 looks like a saw tooth. Once the level reaches 3.2V (±0.3V), the controller shuts down the power converter for a period of time set by the capacitor C17. As R11 = R10 = 300 kΩ and C17 = 4.7 µF, this overload restart delay is about 0.7 seconds. If the overload condition remains (look for a possible short on the output), the power converter will continue to try to come back on-line with 40 ms soft-start every 0.7 seconds. The resulting average current into the short will be very low, less than 0.05 I_{MAX}, where I_{MAX} is set by the value of R16 and turns ratio of T2.

3.1.7 Driving Large Area MOSFETs

Although the output stages of the GP605 are capable of delivering 0.6A peak current, it might be beneficial to use buffer driving stages between the chip and large area MOSFETs. In order to charge 200 pF of gate-source capacitance in 100 ns, the driver stage must deliver up to 0.75 A_{pk} of short current pulses.

It can be achieved by a totem-pole, small signal MOSFET stage, Q3-Q4 (Q5 -Q6). In this case the GP605 output drives only about 70 pF load. Both driver MOSFETs have $R_{DS(ON)}$ of 8 Ω and can provide high current pulses to charge and discharge C_{GS} of power MOSFETs.

3.2 Power Transformer Design

The practical design starts with finding the turns ratio 'n' between the primary winding (1-2) and the secondary windings (3-4) = (4-5) of the power transformer T1.

Assuming low line condition (V = 115V DC for a typical supply), the converter will operate with minimum dead-time (about 25%) and the voltage across the primary will be very close to an ideal sinewave $V_{1\text{-}2} = V \sin \omega_O t$,

$$N = \frac{0.707V}{1.25\,(V_{OUT} + V_F)}$$

Where V_{OUT} is the rectified output voltage and V_F is a forward drop across a Schottky diode.

For V_{OUT} = 5V, V_F = 0.5V, and V = 115V : n ≈ 12

In transformers above 500 kHz, the practical amount of turns for the 5V secondary winding is one turn.
Then (3 - 4) = (4 - 5) = 1 turn and (1 - 2) = 12 turns.
The fundamental relationship in the transformer is:

1. $$e = NA_e \frac{dB}{dt} \quad 10^{-8}$$

Where e is instantaneous voltage across a winding in volts, *N* is the number of turns in that winding, A_e is the transformer core area in cm^2 and dB/dt is the instantaneous rate of change of flux density in gauss per second.

2. $$\Delta B \text{ (over a Time } = \frac{T}{2}) = \frac{10^8}{NA_e} \int_0^{T/2} edt$$

where T is the operating period in seconds.

In the sinewave converter:

3. $$e = E \sin \frac{2\pi}{T} t$$

where *E* = sinewave peak.

4. $$\int_0^{T/2} edt = E \int_0^{T/2} \sin \frac{2\pi}{T} tdt$$

$$= E \left(-\frac{T}{2\pi} \cos \frac{2\pi}{T} \bullet \frac{T}{2} + \frac{T}{2\pi} \cos 0 \right) = \frac{ET}{2\pi}$$

5. $$\text{So } \Delta B = \frac{10^8}{NA_e} \times \frac{ET}{2\pi}$$

From this equation maximum operating flux density can be calculated:

$$B = \frac{10^8 \ V \bullet Tr}{2\pi \ N \bullet A_e}$$

B is in gauss, V is the peak voltage in volts, T_R is the period of resonating frequency in seconds, N = primary turns, and A_e = core area in cm^2.

For Magnetics core F - 43622 - UG,
A_e = 1.59 cm^2 nominal V = 150V. If resonating frequency of 750 kHz is chosen, then

$$B = \frac{10^8 \times 150V \times 1.33 \text{ sec} \times 10^{-6}}{2\pi \times 12 \times 1.59} = 166 \text{ gauss}$$

According to Magnetics Inc. Data, this will result in about 100mW/cm^3 core loss (F material). The 43622 core has a volume of 8.46 cm^3. Total core losses will be approximately 850 mW, quite acceptable for a 125 W transformer.

Winding Losses:
Skin depth can be calculated from this equation:

$$\delta = \frac{0.066}{\sqrt{f}}$$

where δ is in meters, *f* is in Hertz.
For 750 kHz operation δ = 0.076 mm = 3 mils.
In a flat conductor both sides can be considered a surface. So, at 750 kHz frequency, 5 mils of copper foil can be considered a good choice for 1 turn, 25 amperes secondary winding. The average length of turn for this transformer is ALT = 0.244 ft.
Foil width is about 0.5 in.
Foil area is 0.5 in. x 0.005 in. = 0.0025 sq. in.
It is about the same as the area of #16 AWG wire, and it has a resistance of about 4 mΩ per foot. So the resistance of 1 turn of foil is about 1 mΩ. In a full wave secondary winding of this power transformer, one can assume that I_{RMS} (secondary) = 25A and R = 1 mΩ then power dissipation in the foil:
P (secondary) = I^2_{RMS} (sec) x R_{SEC} = 625 mW.
Conservative estimate for I_{RMS} (primary)

$$I_{RMS} \text{ (primary)} = \frac{I_{RMS} \text{ (sec)}}{12\,\eta}$$

where η is the efficiency of the supply (0.75 is the design goal).

Then I_{RMS} (primary) = $\frac{25A}{12(0.75)}$ = 2.78A

The #30 AWG wire would be a good choice for the primary winding; because it has a diameter of only 10mils this wire is quite efficient at 750 kHz.

Due to skin effects however, its DC resistance value has to be multiplied by 1.5 to obtain the true AC resistance at 750 kHz. The DC resistance of #30 wire is 100 mΩ per one foot. So the AC resistance will be 150 mΩ per one foot. Twelve primary turns have the total length of about three feet, therefore total AC resistance value of one strand is 0.45 Ω. Six strands in parallel will have resistance of R_{pri} = 75 mΩ. Then power dissipation in the primary:

$$P_{pri} = I^2_{RMS\ pri} \times R_{pri} = (2.78)^2 \times 0.075 = 580\ mW$$

Total Transformer Power Dissipation

$$P_T = P_{core} + P_{sec} + P_{pri} = 850\ mW + 625\ mW + 580\ mW = 2055\ mW$$

Rule of thumb is that in a well designed switching power supply, total losses in the transformer should not exceed 2% of the output power. In this case 2W transformer losses represent about 1.6% of the output.

The primary winding in this design is split into two halves, each half is 6 turns of 6 strands of #30 wire. The secondary windings are sandwiched between these halves. Such construction greatly reduces the leakage inductance and enhances power conversion.

3.3 Resonating Tank

It is always a challenge to choose the right value for C_r and L_r. If the inductor is too small, the excessive peak currents will make the design inefficient. If the inductance L_r is too high, the amount of power available for conversion will be limited. A good starting point is:

$$P_{OUT} = \frac{C_r V^2_{C peak}}{2} \bullet f$$

$$\text{Then } C_r = \frac{2P_{OUT}}{V_C^2{}_{peak} \bullet f}$$

$f = f_{max}$ = 600 kHz at low line when $V_{c\ peak}$ = 220V

$$\text{Then } C_r = \frac{2 \times 125W}{(220V)^2 \times 600 \times 10^3} = 8608\ pF$$

The closest standard value is 8200 pF. Then L_r can be calculated from the equation

$$L_r = \frac{1}{C_r 4\pi^2 f_r^2}$$

for f_r = 750 kHz L_r = 5.5 µH

3.4 Power Semiconductor Selection

Every bidirectional switch in this supply actually consists of three power semiconductors, a Schottky diode *D2* (or *D3*), a MOSFET *Q1* (or *Q2*), and a fast recovery diode *D4* (or *D5*). The only purpose for *D2* is to block an internal parasitic diode of the power MOSFET. This internal diode is too slow for the purpose. Since the switches *Q1* and *Q2* operate out of phase, the maximum duty cycle for an individual MOSFET is about 38%. That happens at low line and maximum load, when $f = f_{max}$ = 600 kHz.

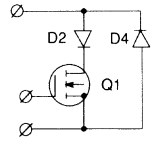


Figure 5

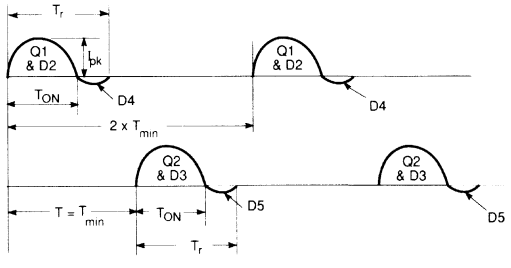


Figure 6

Under these conditions the return current via the diodes *D4* and *D5* almost disappears and peak currents in transistors reach 8A. So, I_{RMS} for *Q1* and *D2* will be the same as for *Q2* and *D3*:

$$I_{RMS\ (MOSFET)} = I_{peak} \sqrt{\frac{T_{ON}}{4T_{min}}}$$

Since $T_{ON} = 0.38\ T_{min}$, $I_{RMS} = 8A \sqrt{\frac{0.38}{4}} = 2.46A$

The power dissipation in every transistor will be limited to conduction losses:

$P_{Q1} = P_{Q2} = (I_{RMS})^2 \times R_{dson}\ (T_j = 100°C)$

For IRFP450 MOSFET; $R_{dson}\ (T_j = 100°C)$

$= 1.7R_{dson}\ (T_j = 25°C) = 1.77 \times 0.4\ \Omega = 0.68\ \Omega$

Then $P_{Q1} = P_{Q2} = (2.46A)^2 \times 0.68\ \Omega = 4.13\ W$

The efficiency can be improved by lowering the MOSFET junction temperature. For example, at 60°C IRFP450 maximum R_{dson} will be 0.52 Ω and losses will drop to 3.15W per transistor.

However, if IRF841 transistor is used, its

R_{dson} (T_j = 60°C) = 1.25 R_{dson} (T_j = 25°C) 1.25 x 0.85 = 1.06Ω

Then $P_{Q1} = P_{Q2}$ = 6.4 watts.

Although it is more efficient to use larger area MOSFETs, economical considerations may dictate the usage of IRF841 but at a lower junction temperature, (less than 60°C).

Schottky diode losses can be calculated from the following equation.

$$P_{D2} = P_{D3} = I_{RMS} \times V_{RMS}$$

where $V_{RMS} = V_{pk}\sqrt{\frac{T_{ON}}{2\,T_{min}}} = V_{pk}\sqrt{\frac{0.38\,T_{min}}{2\,T_{min}}} = 0.436\,V_{pk}$

Assuming $V_{peak} \approx 0.6V$ for a typical Schottky diode, $V_{RMS} \approx 0.26V$, and $P_{D2} = P_{D3} = 0.6$ watts. Return diodes *D4* and *D5* conduct very little current at nominal load. Only at light loads do they conduct significant current, and then, the duty cycle is very low. Although these diodes must be rated for up to I_{Q1peak} currents, they dissipate little power, approximately 0.5W each. Diodes must have 35ns - 50ns recovery time, so, $P_{D4} = P_{D5} \approx 0.5$ watts. Each power switch loss = $P_{Q1} + P_{D2} + P_{D4} = 6.4W \approx 0.5W = 7.5$ watts. Both switches (six semiconductors) dissipate 15 watts.

OUTPUT SCHOTTKY

$P_{D12} + P_{D13}$ = 25A x 0.55V = 14 watts. Switching losses are low due to the sinusoidal character of the current.

3.5 Snubbers

These RC networks across power switches are needed to dampen voltage spikes. They reduce EMI and improve reliability.

Power losses:

$$P_{R4} = P_{R5} = \frac{C_5 V^2_{C5}}{2} \times \frac{f_{max}}{2} = \frac{47 \times 10^{-12}(220)^2}{2} \times \frac{6 \times 10^5}{2}$$

= 0.340W (low line, nominal load), total losses are 0.7W

It should be noted that at nominal line, snubber losses will be higher because they are proportional to V_C^2. For example, at nominal line

V_C = 300V and f = 350 kHz, then $P_{R4} = P_{R5}$ = 0.74 watts. Total losses will be 1.5 watts.

3.6 Power Supply Efficiency

Power switch losses	15.0W
Output Schottky diode losses	14.0W
Losses in snubbers	1.5W
Power Transformer losses (est)	2.0W
Control/drive circuits	1.0W
Output inductor dissipation (est)	2.0W
Resonating inductor dissipation (est)	0.5W
Input rectifier dissipation (est)	3.0W
TOTAL LOSSES	39.0W

Estimated efficiency $n = \frac{125W}{164W} \times 100\% = 76.2\%$

Measured efficiency $n = \frac{125W}{167W} = 74.8\%$

Additional losses totalling 3W are miscellaneous losses in device leads, printed circuit board etches, and proximity effect losses in the power transformer etc. A target for an off-line 5V output switching power supply is 75% efficiency.

3.7 Possible Modifications to the Power Supply

This topology can be easily modified to achieve multiple output units. Additional windings can be placed on the power transformer as long as the total power does not exceed the rated value. Higher power supplies would require modification in the switches, transformers, as well as in the resonating tank. Output stages also would have to be *beefed-up*. The control circuit would require very minor modifications in the areas of current sensing and the compensation network.

4.0 PERFORMANCE ANALYSIS

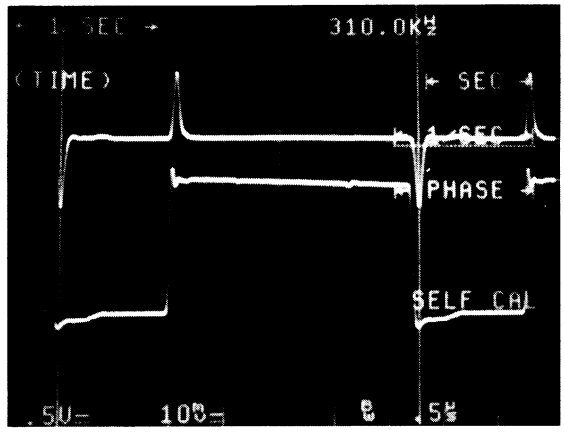
Among the most important characteristics of a power supply, are: efficiency, line and load regulation, transient response, and output ripple. The measured efficiency of the GP605 supply was approximately 75%. Line regulation (95V AC to 132V AC) was better than ±0.5 percent. Load regulation (5% to 100%) was better than ±1.5 percent. Total regulation band was better than ±2 percent. Transient response for 50% - 100% load-step was an excursion of less than ±5% of the output voltage, with total recovery under 500µs. Output ripple was less than 100 mV p-p.

All the above characteristics are quite acceptable for an off-line switching power supply.

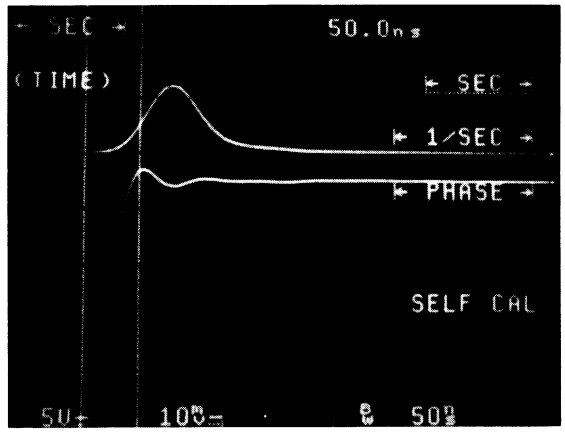
5.0 WAVEFORMS

Figure 7 shows the GP605 output driving totem-pole signal MOSFETs. Figure 8 shows the actual power supply resonating current versus GP605 outputs.

Fig. 7 Output Stage Driving Totem-pole MOSFETs
V_{CC} = 12V DC

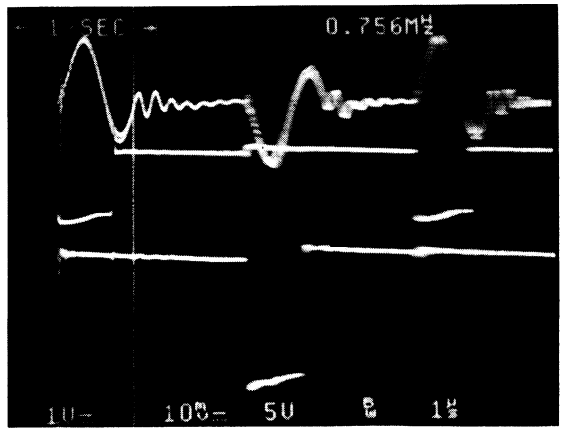


a) 0.5μs/div
Output Current 100mA/div
Output Voltage 5V/div



b) 50 ns/div

Fig. 8 Oscillograms of GP605 Output Stage Voltage and Power Transformer Current



Upper trace:
Power Transformer Primary Current
5A/div
1μs/div
Middle trace:
Drive A Voltage 10V/div
Lower Trace:
Drive B Voltage 5V/div

6.0 CONCLUSION

THhe GP605 provides an easy and cost effective way to control and protect resonant and quasi-resonant converters. The lack of suitable FM controllers has stopped many designers in the past from going to new topologies and higher frequencies, - now they have a choice.

References:

(1) Neville Mapham, "An SCR Inverter with Good Regulation and Sine-Wave Output," IEEE Trans. on Industry and General Applications, Vol.IGA-3, pp. 176-187, March/April 1967.

(2) Alex Estrov, "Power Transformer Design for 1MHz Resonant Converter" Proc. First High Frequency Power Conversion Conference" April 1987, Intertec Communications, Ventura,California.

(3) N.O. Sokal and A.D. Sokal, "Class E - a new class of high-efficiency tuned single-ended switching power amplifiers," IEEE J.Solid-State Circuits, vol. SC-10, no. 3, pp. 168-176, June 1975.

(4) Alex Estrov, Iain Scott, "FM Controller IC Supports up to 1 MHz Resonant supplies" PCIM, September 1987,Intertec Communications, Ventura, California.

RESONANT POWER SUPPLY BILL OF MATERIALS

C1, C2	Capacitoral.el. 330 µF 200V
C3, C4	Capacitor met.polyprop. 1µF 200V
C5, C6	Capacitor cer.NPO 47pF 1kV
C7	Capacitor cer.NPO 8200 pF 1kV
C8,C10,C11,C18,C30	Capacitor cer. X7R 0.22 µF 25V
C9, C31	Capacitor tant.conformally coated 4.7µF 35V
C16, C17, C21, C27	Capacitor tant.conformally coated 4.7uF 16V
C12, C13, C14, C15	Capacitor tant.conformally coated 220 µF 10V
C19, C24	Capacitor cer. X7R 0.022 µF 25V
C20, C26	Capacitor cer. NPO 1000 pF 25V
C22	Capacitor cer. NPO 150 pF ±5% 25V
C23	Capacitor cer. NPO 100 pF ±5% 25V
C25	Capacitor cer. X7R .047 µF 25V
C28, C29	Capacitor film 1000pF 250VAC 'Y' type
D1	Diode bridge 4A 600V Gen. Instr. KBU4J
D2, D3	Diode Schottky IN5823
D4,D5	Diode UFRD Amperex BYV29-500
D7	Diode IN4001
D8,D9	Diode UFRD Motorola MUR105
D10, D11, D14	Diode IN4148
D12, D13	Diode Schottky Motorola MBR3045PT (each)
D15	DiodeZener IN967A
F1	Fuse 5A 250VAC slo.blo.
L1	Inductor 5 µH ±5%, Core:Micrometals T51-8/90 12 turns of #28 AWG
L2	Inductor 7.5 µH ± 10%. Core: Arnold Eng. A-445146-2 or Magnetics 55344-A2. 7 turns of 5 strands in parallel #20 AWG.
L3	Inductor 330 µH, 85 ma. TDK EL0606 SKI-331K
Q1, Q2	MOSFET IRF840
Q3, Q5	MOSFET Supertex VP0104N3 P-channel 8 Ω
Q4, Q6	MOSFET Supertex VN1306N3 N-channel 8 Ω
R1	Thermistor NTC 3A Ametek SG220
R2, R3	Resistor 33 kΩ 5% 0.25W
R4, R5	500 Ω 10% 1W Corning FP1
R6	Thermistor PTC 3 kΩ Midwest 220Q32214
R8, R9	Resistor 100 kΩ 5% 0.25W
R10, R11	300 kΩ 5% 0.25W
R12	360 kΩ 1/2W 400V
R13, R18	3 kΩ 5% 0.25W
R14	17.4 kΩ 1% .25W
R15	240 Ω 5% 0.25W
R16	56 Ω 5% 0.25W
R17	10 k Ω 5% 0.25W
R19	9.31 kΩ 1% 0.25W
R20	1 MΩ 5% 0.25W
R21, R22	470 Ω 5% 0.25W
R23	910 Ω 5% 0.25W
R24	1 kΩ 5% 0.25W
R25	Trim pot. 200 Ω
R26	Resistor 20 k Ω 5% 0.25W
T1	PWR.Transformer. Core: Magnetics DF43622-UG. (1-2) = 12 turns of #30 AWG, six strands in parallel, split 6 turns + 6 turns. (3-4) = (4-5) = 1 turn of 0.005" copper foil, *sandwiched* between two halves of the primary (1-2). (6-7) = (7-8) = 3 turns of #30 AWG
T2	Transformer, current sense. Core: Magnetics 40705-TC-F (1-2) = 1 turn of #28 AWG (3-4) = 40 turns of #32 AWG
T3	Transformer, gate drive. Core: Magnetics 40705-TC-F. (1-2) = (3-4) = 20 turns of #32, double insulated wire, wound bifilar.
U1	Linear Regulator LM78M12
U2	FM Controller Gennum GP605
U3	Optocoupler Motorola MOC604A
U4	Shunt Regulator TI 431CLP

REVISION DATE MAY, 1990

The GP605 in a Variable Frequency, Zero Current Switching, Forward Mode Resonant Mode Power Supply

APPLICATION NOTE

1.0 INTRODUCTION

Conventional quasi-square wave converters, mostly PWM controlled, have been very effective tools for power supply designers for quite a few years. Their most natural operating frequencies are between 20 kHz to 200 kHz. Lately,in the search to reduce size and cost, these converters are approaching the 500 kHz region, which is exotic for this topology. Recent developments in high frequency magnetics materials and high frequency capacitors make it possible to operate even in the high frequency region up to 1 MHz. This allows about a 3:1 reduction in the size of major passive components, as compared to 20 kHz switchers.

The biggest disadvantage for SMPS converters at these frequencies is high switching losses in power semiconductors. The resulting inefficiency requires larger heat sinks and thus defeats the goal of reducing the size.

There is, however, a more efficient way to convert power at ever higher frequencies. This class of converters is called "resonant" and can implement a zero current switching or zero voltage switching technique. A sinusoidal waveform can be generated either by a parallel or series resonating LC tank.

The clear advantage of the sine waveform is that switching generally occurs at zero crossing and switching losses in power semiconductors are almost eliminated or greatly reduced. The primary disadvantage of a resonant converter is that, for a given power level, the actual peak current is three to four times greater than that of a PWM converter. This can be overcome by using in some topologies fast SCR or, in general, by using low "on resistance" semiconductors. This creates a practical means to increase operating frequencies up to 1 MHz and higher. High frequencies allow designers to achieve power densities in excess of 25 W/cubic inch, which is about four times better than is possible at 100 kHz.

There are many types of resonant and quasi-resonant topologies. If you are interested in a brief review of some of these topologies, request the article published in IEEE Spectrum magazine, " *Resonant Mode Power Supply Design: A Primer* " by Fred Sykes , Gennum Corporation.

In this application note you will find a description of the zero current switching topology in variable frequency mode. An FM control type provides a fixed "*on time*" (T_{ON}),and variable frequency (f). Conversely PWM uses fixed period and variable on "*time*".

This paper describes features and applications of the GP605 resonant mode controller in one type of resonant power supply. The GP605 is an upgraded version of the LD405, which was the first commercially available resonant mode controller.

2.0 GP605 BLOCK DIAGRAM

Figure 1 shows a functional block diagram of the GP605. The heart of this IC is a voltage controlled oscillator (*VCO*) and a monostable. The *VCO* sets a variable commutating frequency, while the monostable sets a fixed T_{ON} time.

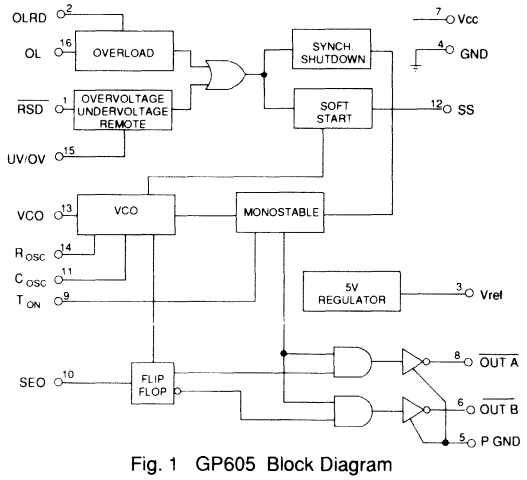


Fig. 1 GP605 Block Diagram

The IC can work either in a single-ended, or in a push-pull mode. Grounding pin 10 (*SEO*) enables a "*steering*" flip-flop to control the output AND gates, thus sending the drive to *OUT A* and *OUT B* in a push-pull mode. Opening pin 10 puts the chip into single-ended operation. In this mode the frequency is doubled compared to individual outputs in push-pull mode. The outputs are identical, so they can be paralleled for increased drive capability. T_{ON} time is independent of the mode of operation.

The chip has an overvoltage/undervoltage (*OVUV*) window comparator, the threshold of which can be set externally.

A soft-start block allows relatively slow frequency change, (usually measured in tens of milliseconds) from minimum *VCO* frequency to the value set by the *VCO* input pin 13. The soft-start initiates with every power-on of the chip, as well as after any forced shutdown.

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Shutdown can be achieved by grounding the remote shutdown pin 1 (*RSD*), by applying on pin 15 (*OVUV*) a voltage outside of the window comparator, or by applying a voltage level in excess of 3.2 V to the overload input pin 16 (*OL*).

Every shutdown of the GP605 is synchronous with the monostable, meaning that the controller never interrupts the T_{ON} in the middle of the pulse. This feature is especially suited for resonant power supplies, since resonant cycle interruption might cause excessive voltage spikes. These high dv/dt spikes could damage switching semiconductors, especially power MOSFETs. It is much safer to allow the cycle to elapse, and then to shut down the converter.

Every time the overload block shuts down the chip, it does so for 0.5 to 2 seconds resulting in a "*hiccup*" mode of overload protection. The exact timing is set by an external capacitor on pin 2 (*OLRD*). Such overload protection effectively "*folds back*" output on any prolonged overload or short. The converter will still have an automatic recovery once the voltage on *OL* pin drops below the threshold level.

3.0 RESONANT CIRCUIT THEORY OF OPERATION

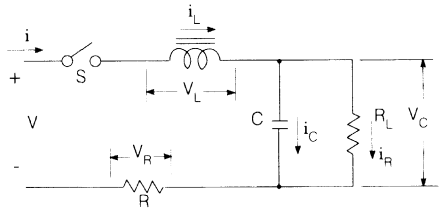

Fig. 2

In the circuit which consists of *L*, *C*, *R* and R_L, there is a commutating switch *S*. Its function is to apply DC voltage of a known source *V* to a series resonating tank *LC*. Resistor R_L represents a load and "*steals*" some current from the tank. Once the resonant process is finished, the switch *S* is opened interrupting the power conversion from the source *V* to the resistor R_L. After a time interval, switch *S* is closed and the process repeats itself. One can change the commutating frequency, thus changing the average power being dissipated in the resistor R_L. If *L*, *C* and *S* were ideal components (which they are not), there would be no power dissipated anywhere, except into the load R_L and resistor *R*.

Let us first assume that $R_L = \infty$

$$i = i_L = i_C + i_R \qquad (1)$$

$$V = V_L + V_C + V_R = L\frac{di}{dt} + \frac{1}{C}\int i_C\,dt + i \bullet R \qquad (2)$$

The LC circuit has resonant conditions when:

$$X_L = X_C \qquad (3)$$

$$\text{i.e. } \omega L = \frac{1}{\omega C} \qquad (4)$$

Resonant frequency $\omega_O = 2\pi f_O$ can be determined from the expression:

$$\omega_O = \frac{1}{\sqrt{LC}} \qquad (5)$$

Impedance of resonating tank *Z* at the frequency ω_O:

$$Z = \omega_O L = \frac{1}{\omega_O C} = \sqrt{\frac{L}{C}} \qquad (6)$$

Ratio of reactive voltage V_L or V_C to the real voltage V_R, is called Quality factor *Q*:

$$Q = \frac{V_L}{V_R} = \frac{V_C}{V_R} = \frac{Z \bullet i}{R \bullet i} = \frac{Z}{R} \qquad (7)$$

Quality factor *Q* shows how many times voltage across inductor or across capacitor will exceed the source voltage *V*.
Let us determine the sum of the energy of magnetic and electric fields in the tank:

$$W = W_{mag} + W_{electric} \qquad (8)$$

current in the tank: $i = I_{peak} \bullet \sin \omega_O t \qquad (9)$

Then

$$V_C = V_{Cpeak} \bullet \sin\left(\omega_O t - \frac{\pi}{2}\right) = -V_{Cpeak}\cos\omega_O t \qquad (10)$$

$$W = W_{mag} + W_{electric} = \frac{L i^2}{2} + \frac{C V_c^2}{2}$$

$$= \frac{L I^2_{peak}}{2}\sin^2\omega_O t + \frac{C V^2_{Cpeak}}{2}\cos^2\omega_O t \qquad (11)$$

$$\text{But } V_{Cpeak} = \frac{1}{\omega_O C} \bullet I_{peak} = I_{peak}\sqrt{\frac{L}{C}} \qquad (12)$$

$$\text{So } \frac{C V^2_{Cpeak}}{2} = \frac{L I^2_{peak}}{2} \qquad (13)$$

$$\text{Then } W = W_{mag} + W_{electric} = \frac{L I^2_{peak}}{2} = \frac{C V^2_{Cpeak}}{2} = \text{const}$$

i.e. the sum of the magnetic fields does not change in time. The decrease in the electric field is compensated by the increase in the magnetic field and visa versa. Thus a constant conversion of the magnetic field into the electric field and back again is taking place.

The power dissipation takes place only in the resistor *R*. If the switch *S* is turned on for a period of time:

$$T_O = \frac{1}{\omega_O} = \frac{1}{2\pi f_O}$$

one complete resonant cycle will take place with power loss in the resistor *R*.

$$P = (I^2_{RMS}) \bullet R \qquad (14)$$

Differential equations for the circuit in Figure 2 are well known. The solutions are:

$$V_C = V + \frac{V}{\omega_O \sqrt{LC}} \bullet e^{-\frac{Rt}{2L}} \bullet \sin\left(\omega_O t + \frac{\pi}{2}\right) \qquad (15)$$

$$i = \frac{V}{\omega_O L} \bullet e^{-\frac{Rt}{2L}} \bullet \sin\left(\omega_O t\right) \qquad (16)$$

$$V_L = \frac{V}{-\omega_O \sqrt{LC}} \bullet e^{-\frac{Rt}{2L}} \bullet \sin\left(\omega_O t - \frac{\pi}{2}\right) \qquad (17)$$

The resulting waveforms are shown in Figure 3. Voltage V_C is circulating around the source voltage *V*. It cannot exceed *V* multiplied by 2. This voltage reaches its maximum point around $\frac{T_O}{2}$

The current is also circulating, although around zero.

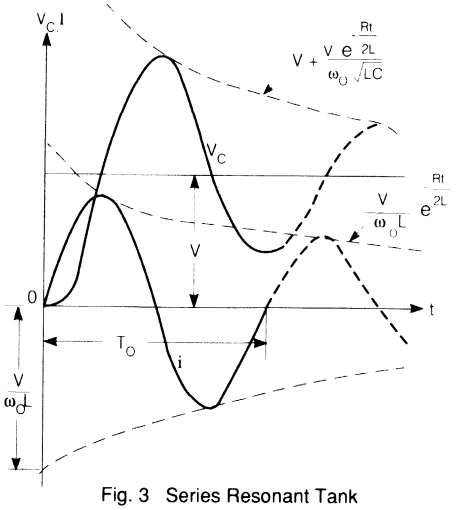

Fig. 3 Series Resonant Tank

For an ideal tank R = O

$$V_C = V - V \cos \omega_O t \qquad (18)$$

$$i = \frac{V}{\sqrt{L/C}} \sin \omega_O t \qquad (19)$$

$$V_L = V \cos \omega_O t \qquad (20)$$

This means that the resonating process would continue indefinitely. In the case of R_L being connected across capacitor *C*, the load will see an AC voltage V_C across it and thus will dissipate power. In practice, circuit R_L is connected to the tank via an isolation power transformer. The new value R_L' is then

$$R_L' = n^2 R_L, \text{ where } n = \frac{N_{pr}}{N_{sec}} \text{ is the turns ratio.}$$

4.0 RESONANT POWER SUPPLY

A block diagram of a parallel resonant converter is shown in Figure 4 . The detailed schematic diagram of this supply is shown in Figure 9.

An input circuit provides filtered DC bus voltage for the high frequency resonant converter. In the case described in this paper, the input circuit consists of input capacitors *C2, C3*.

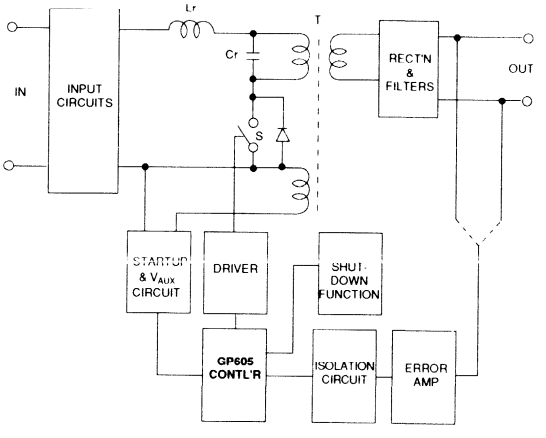

Fig. 4 Block Diagram of a Parallel Resonant Converter

The startup circuit provides energy for circuit operation at the time *T* = 0. Startup energy is supplied by current source *Q2*. The GP605 is in the OFF condition if voltage is below 9 V (typical). Once the power supply is up and running, energy is taken from the power transformer auxiliary winding *T2*.

The voltage from the winding is rectified (*CR8, CR7*) and regulated (*VR1*) to the level of 12 V. If the startup current is too high for your application please request the GP6040 data sheet 510-59. The GP6040 features very low startup current.

A resonating series tank consists of an inductor *L2* and capacitors *C4,C32*. The load is connected in parallel to the resonant capacitor via stepdown transformer *T2*. This type of converter, following old RF definition is called parallel resonant converters, despite the series resonant circuit.

The GP605 delivers constant "on" time to the switch and voltage regulation is achieved by frequency variation. Switch *Q1* is "on" for a period of time long enough for half of the full resonant cycle. A parallel diode to the switch provides a return path for the resonant current.

In order to provide fast turn-on and turn-off of the power switch Q1, driving requires an additional stage. This is achieved by using MOSFET transistors (*Q3, Q4*) in a totem-pole circuit configuration. Such an approach limits controller power dissipation and therefore increases product reliability.

The error amplifier in this particular application is designed on the secondary side. The error signal is transmitted to the primary via optocoupler *U2* and applied to the Voltage Control Oscillator (*VCO* input) pin 13.

The soft -start function is controlled by capacitor *C16* connected to pin 12. The controller of $T = 0$ applies minimum frequency to the circuit. The rate of frequency increase is controlled by capacitor *C16*. The frequency increases until it reaches the value set by the error amplifier.

The supply utilizes primary current sensing. Current sensing transformer *T1* is connected in series with the power transformer *T2*. The transformer has the turn ratio 1 : 50. On the secondary side the voltage signal is linearly proportional to the current on the primary side of the current transformer (*CT*). After rectification and some filtering, an essentially "*saw tooth*" voltage level is applied to pin 16 of the controller. Once the signal reaches a programmed threshold, the controller shuts down for approximately 1 sec. The period is set by capacitor *C11* connected to pin 2. When time elapses the GP605 applies a normal pulse train, beginning from lowest frequency, as during soft-start function. If overload is still present the circuit goes to shutdown mode again. The supply will stay in the "*hiccup*" mode until the overload is removed.

The output stage is a fairly straightforward design. It is a full-wave Schottky, center-tap rectifier, composed of *CR10, CR11, L3* and a row of output capacitors.

5.0 DESIGN SEQUENCE

5.1 Integrating the GP605 in the Power Supply

5.1.1 Maximum and Minimum VCO Frequency ($f_{min/max}$)

The maximum operational frequency of the GP605 is 2 MHz. However usable frequency is limited by the *dead time* introduced internally to the end of each T_{ON} time, to prevent overlapping of the complementary outputs.

Since energy conversion takes place only during T_{ON} time, the limitation in D_{max} (duty cycle) lowers the practical maximum frequency (f_{max}). Table 1 gives useful information on T_{ON}, f_{max} and D_{max} for single-ended operation.

f_{max}	2000	1500	1000	600	500	400	kHz
T_{ON}	200	366	700	1366	100	2200	ns
D_{max}	40	55	70	82	85	88	%

Table 1.

If your application requires a high duty cycle in the 3 MHz frequency range, request GP6050, or GP6040 data sheets (documents 510-58 and 510-59 respectively, avail. Fall '89).

In this design f_{max}, is set at 510 kHz. A reasonable capacitor value from the noise point of view is 100 pF. For a 100 pF capacitor, from Figure 5 on GP605 data sheet, the minimum frequency is 12 kHz. From Figure 6 on the same data sheet, oscillator resistance is 26 kΩ.

Recommendations for oscillator components are:
- *C17* (oscillator capacitor) ceramic, temp. coef. NPO, 100 pF
- *R14* (oscillator resistance) metal film, 1%, 26.1 kΩ.

Tolerance of f_{max} from chip to chip is 5% (484 kHz to 536 kHz).

5.1.2 Set Output Pulse Width T_{ON}

The chosen resonant frequency is f_r = 600kHz. The T_{ON} pulse initiates the resonant cycle. The pulse must be terminated during conduction of the diode *CR3* (negative voltage on switch *Q1*). The best way to terminate the T_{ON} pulse is right in the middle of a negative half of the sinewave current:

$$T_{ON} = 0.75 \frac{1}{f_r}$$

From the above equation T_{ON} = 1250 ns. To limit the number of parts used in design, the value of the timing capacitor(*C18*) is equal to the oscillator capacitor, *C18* = 100 pF.

From Figure 2 on the GP605 data sheet (510-43) the timing resistor *R16* = 10 kΩ. A metal film, 1% resistor is recommended.

5.1.3 Soft-start Capacitor

This capacitor is connected to pin 12 and provides controlled startup from f_{min} to f_{max}. Startup requirements vary from application to application; for 100 W power level, a delay of 40 ms is chosen. The delay is approximately equal to:

$$T_{del}\ [ms] = 8.7 \times C\ [\mu F]$$

From the above, capacitor *C16* = 4.7μF

For a 500 W supply a delay time of 200 ms could be used.

5.1.4 VCO Input

In this design the *VCO* input voltage is set by an error amplifier via an optocoupler.

The proper level of the current in the photo transistor is set by an external resistor *R15* parallel to an internal 10 kΩ resistor. To achieve a *VCO* input level of 3.8 V (middle of the *VCO* range) *R15* = 3.9 kΩ.

5.1.5 Overload protection (OL)

Current sensing is provided by current transformer *T1*. Current on secondary side of the transformer is reduced by a factor of 50. After rectification and filtering, the voltage across capacitor *C13* is applied on pin 16. Once the level reaches 3.2V, the controller shuts down the power converter. The period of time the converter is shutdown is adjusted by capacitor *C11*. To achieve current limiting of 0.05 I_{max}, it is necessary to obtain restart every 1 s with additional 40 ms soft-start feature. From Figure 1 on the GP605 data sheet (510-43), *C11* = 4.7 µF and *R6* = *R7* = 300 kΩ (resistance on Figure 1 represents the parallel connection of *R6* and *R7*).

5.1.6 Driving Large Area MOSFETs

The GP605 is capable of delivering 0.6 A current in short pulses, but by using this feature it is very easy to exceed the maximum power dissipation of the package. Increased temperature of the chip will usually decrease reliability numbers. In this design the power MOSFET is driven by the totem pole small signal MOSFET stage *Q3*, *Q4*. The GP605 is driving only approximately 70pF load. Great care must be taken to prevent the voltage on the output pins from going below ground potential, or more than 0.5V above V_{CC}.

5.2 Power Transformer

Calculation of the power transformers for 500 kHz frequency range always causes a great challenge to the designer. The best choice is probably to use standard or custom made planar magnetics, whose electrical characteristics are best suited for a high frequency environment. Refer to (2) and (5) in the reference section.

If, for development purposes, it is required to design power magnetics for that high frequency, some useful information is presented in our application note 510-62 (Half Bridge Resonant Power Supply).

5.3 Resonating Tank

A very important part of the design is to choose the proper value of the resonant capacitor and resonant inductor. Too small an inductor creates high current peaks, too large an inductor leaves a small amount of power available for conversion.

A good starting point to choose the resonant tank capacitor is the output power estimation:

$$P_{OUT} = \frac{C_r \times V_{C\,peak}^2}{2} \times f$$

then

$$C_r = \frac{2 \times P_{OUT}}{V_{C\,peak}^2} \times \frac{1}{f}$$

$f = f_{max} = 510$ kHz

$P_{OUT} = 100$ W

$V_{Cpeak} = 72$ V

The calculated value of the capacitor is 0.0756 µF.

The iteration process to limit size, current peaks, and inductor size limits selected resonant capacitance to 0.044 µF.

The inductor can be calculated from equation

$$L_r = \frac{1}{C_r \times 4 \times \pi^2 \times f_r^2}$$

$f_r = 600$ kHz

Resonant inductor *L2* = 2.2 µH.

5.4 Power Semiconductor Selection

Used in this application the bilateral or fullwave switch consists of three major components, the MOSFET transistor *Q1*, the fast recovery diode *CR3* and the Schottky diode *CR1*. Transistor *Q1* is the main switching device and has a high requirement for maximum peak current. The Schottky diode *CR1* prevents the MOSFET parasitic diode from conducting (too slow for the purpose). The fast recovery diode *CR3* conducts to return resonant current.

Under maximum load condition the return current almost disappears and the peak current in the transistor can be calculated from

$$I_{peak} = \sqrt{\frac{2 \times P_{IN}}{L_R \times f_{max}}}$$

Peak current $I_{peak} = 14.7$ A

Then transistor RMS current

$$I_{RMS} = I_{peak} \sqrt{\frac{f_{max}}{4 \times f_r}}$$

RMS current $I_{RMS} = 6.8$ A

The power dissipation in resonant mode converters is limited mainly to conduction losses.

For IRFP250

$$P_{dt} = (I_{RMS})^2 \times R_t \ (T_{amb} = 100\ ^\circ C)$$

$$P_{dt} = (6.8\ A)^2 \times 0.136 = 6.29\ W$$

The transistor requires very efficient cooling.

Schottky diode losses can be calculated from the following equation.

$$P_{SH} = I_{RMS} \times V_{RMS}$$

where

$$V_{RMS} = V_{peak} \sqrt{\frac{f_{max}}{4 \times f_r}}$$

Assuming V_{peak} = 0.6 V and I_{RMS} = 6.8 A, power dissipation on the Schottky diode is P_{SH} = 1.89 watts.

The return diode *CR3* conducts very little current at nominal load. Only at light loads will the diode conduct significant current, and then, the duty cycle is very low. The diode must be rated up to the transistor peak current. The power dissipation of this component is approximately 1 W. The total power dissipation for the bilateral switch is:

$$P_D = 6.29 + 1.89 + 1 = 9.18\ W$$

5.5 Snubbers

Snubber calculation is done as for a normal PWM converter.

The power loss on the resistor is

$$P_{PS} = \frac{C5 \times V_{max}}{2} \times f_{max}$$

$C5 = 680$ pF

$V_{max} = 100$ V

$f_{max} = 510$ kHz

The total snubber losses are P_{PS} = 1.74 watts.

5.6 Power Supply Efficiency

Power switch losses	9.2 watts
Output Schottky diode losses	11.0 watts
Losses in snubbers	1.8 watts
Control/drive circuits	0.5 watts
Power transformer losses (est)	2.0 watts
Output inductor dissipation (est)	2.0 watts
Resonating inductor dissipation (est)	0.5 watts
Miscellaneous losses	3.0 watts
TOTAL LOSSES	30.0 watts

$$\text{Estimated efficiency} = \frac{100\ W}{130\ W} \times 100\% = 78\ \%$$

Measured efficiency = 81 %

5.7 Possible Modifications to the Power Supply

This topology can be easily modified to achieve multiple outputs. Additional windings can be placed on the power transformer as long the total power does not exceed the rated value. If your application requires half bridge topology please request Application Note 510-62.

6.0 PERFORMANCE ANALYSIS

Efficiency	80%
Line regulation 36V to 60V	±0.1%
Load regulation 2A to 20A	±0.5%
Output ripple	33 mV

7.0 WAVEFORMS See next page

REFERENCES:

(1) Neville Mapham, "An SCR Inverter with Good Regulation and Sinewave Output", IEEE Trans. on Industry and General Applications Vol. IGA-3, pp. 176-187, March/April 1967.

(2) Alex Estrov, "Power Transformer Design for 1 MHz Resonant Converter", Proc. First High Frequency Power Conversion Conference, April 1987, Intertec Communications, Ventura, California.

(3) N.O. Sokal and A.D. Sokal, "Class E - a new class of high efficiency tuned, single-ended switching, power amplifiers", IEEE J. Solid-State Circuits, vol. SC-10, no. 3 pp. 168-176, June, 1975.

(4) Alex Estrov, Iain Scott, "FM Controller IC Supports up to 1 MHz Resonant Supplies", PCIM, Sept. 1987, Intertec Communications, Ventura, California.

(5) "The GP605 in a Variable Frequency, Zero Current Switching, Half Bridge, Resonant Power Supply", Gennum Corporation, Application Note 510-62

Fig. 5 Resonant Supply Waveforms

Upper trace: VDS 50V / div
Middle Trace: I_{TANK} 5A / div
Lower Trace: VGS 5V / div
at V_{IN} = 48 V
1 µs / div

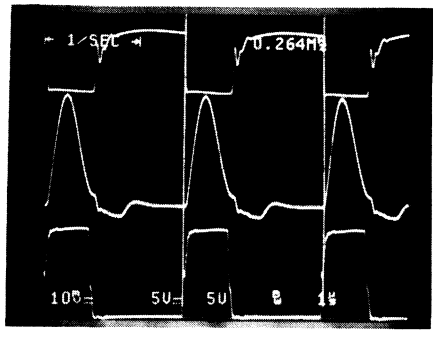

Fig. 5a. I_{OUT} = 20 A

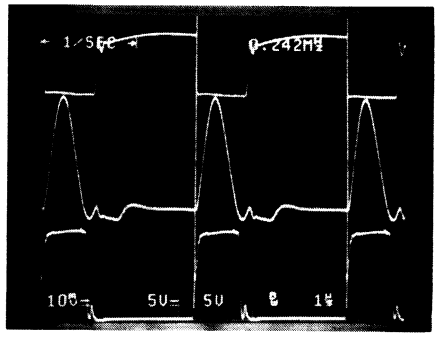

Fig. 5b. I_{OUT} = 15 A

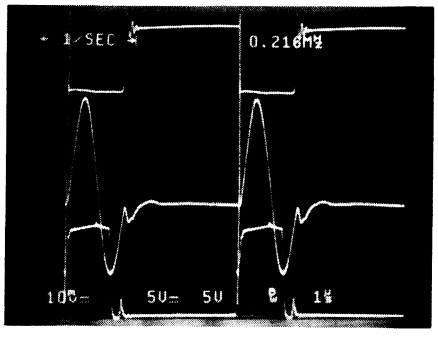

Fig. 5c. I_{OUT} = 5 A

Fig. 6 Resonant Supply Waveforms

Upper trace: VDS 50V / div
Middle Trace: I_{TANK} 5A / div
Lower Trace: VGS 5V / div
at I_{OUT} = 20 A
1 µs / div

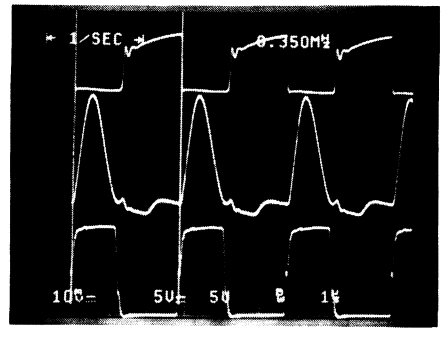

Fig. 6a. V_{IN} = 36 V

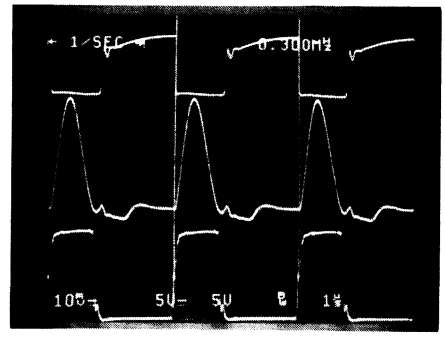

Fig. 6b. V_{IN} = 40 V

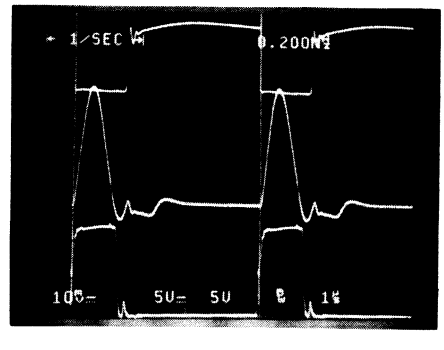

Fig. 6c. V_{IN} = 60 V

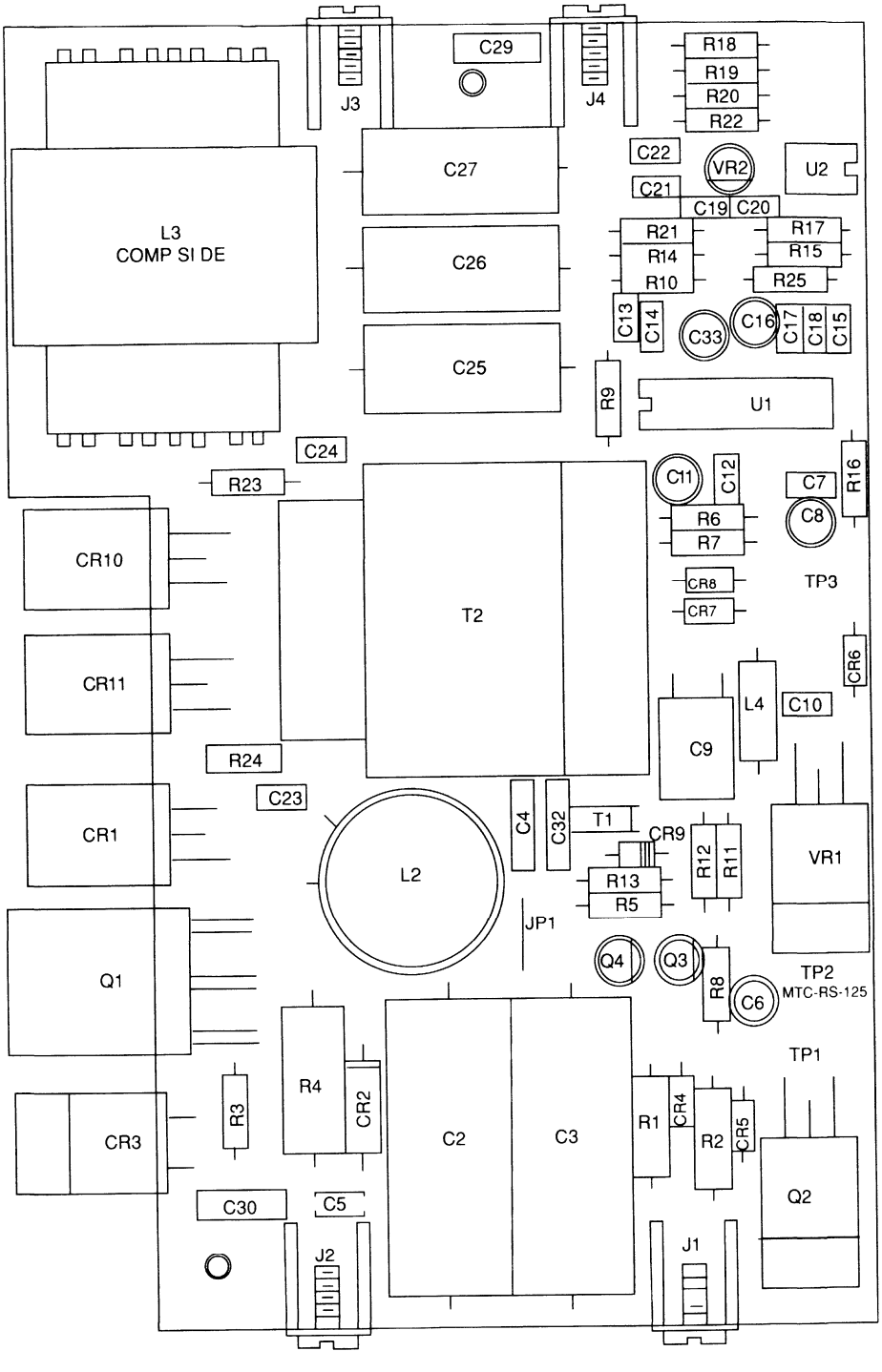

Fig. 7 PCB Layout of Resonant Converter 48V / 5V at 20 A

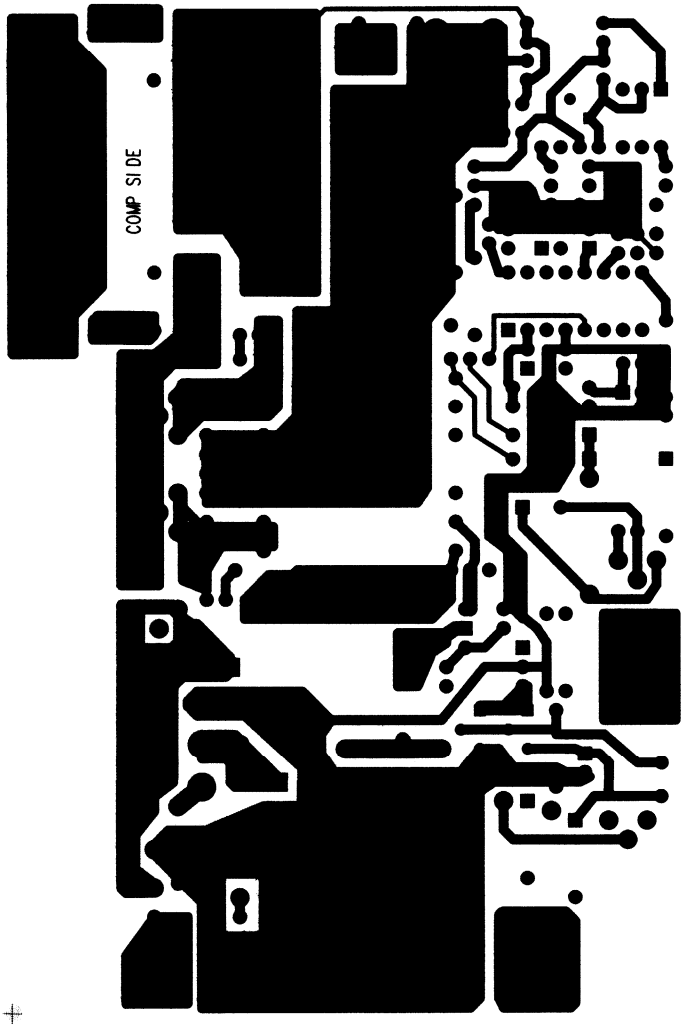

Fig. 8 Component Side of the Resonant Converter 48V / 5V at 20 A

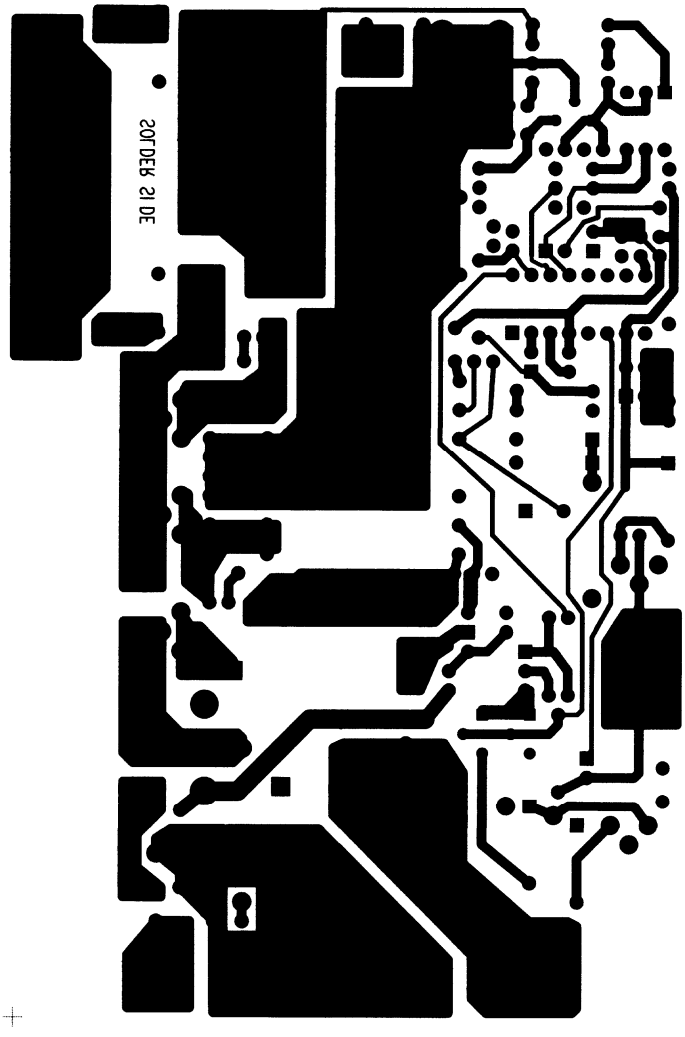

Fig. 8 Solder Side of the Resonant Converter 48V / 5V at 20 A

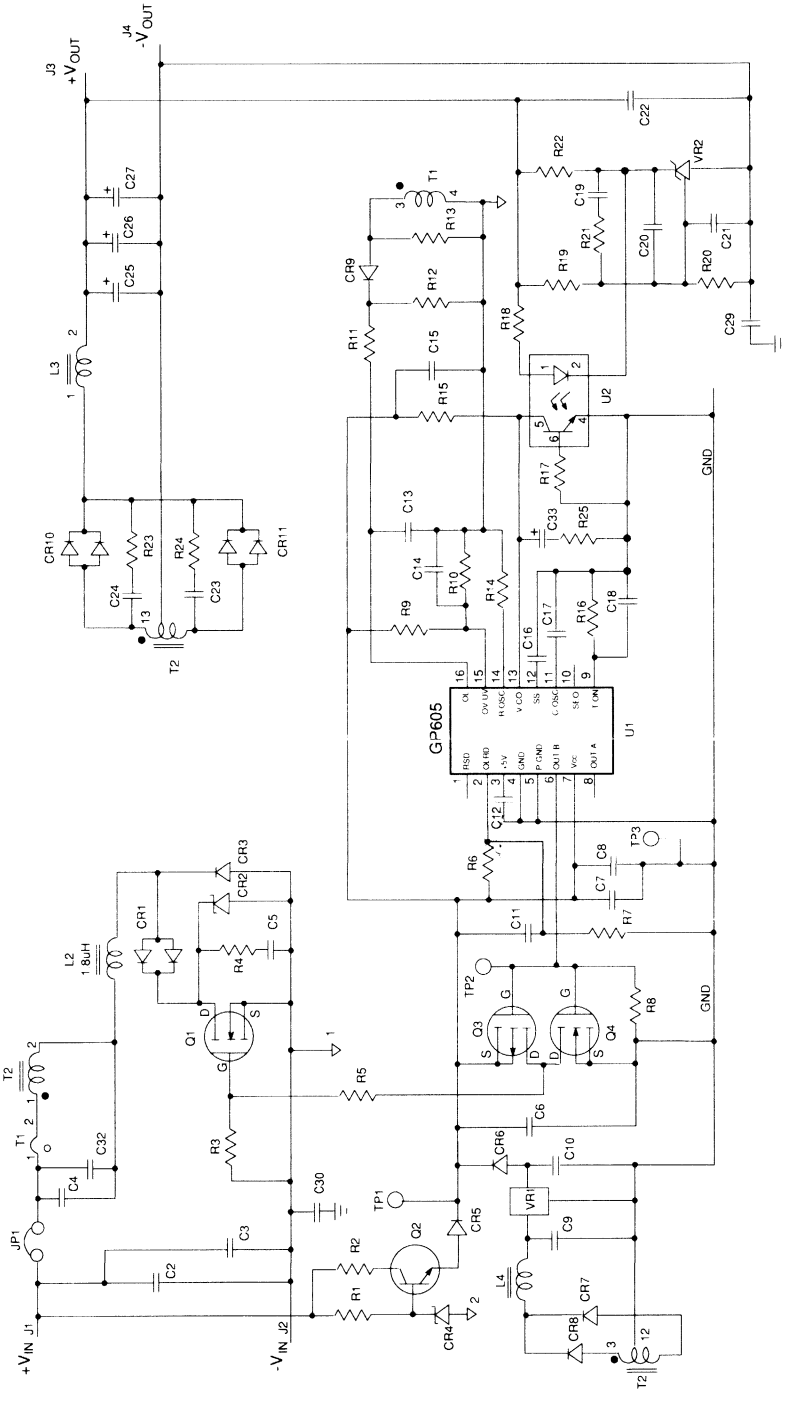

Fig. 9 Schematic of Resonant Converter 48V / 5V at 20 A

RESONANT MODE POWER SUPPLY
BILL OF MATERIAL

Part No.	Description
C2,C3	6.0µF 100V ±10% Electrocube 230BIB605k
C4,C32	0.022µF 200V NPO ±5% KEMET C340C223J2G5CA
C5	680pF 200V NPO (COG) ±5% KEMET C323C681J2G5CA
C6,C8	22µF 16V tant. dipped cap. Sprague 199D226X9016DA1
C7,C10,C15,C19,C20,C22	0.22µF 50V Z5U ±20% Sprague 1C10Z5U224M050B
C9	47µF 20V tant. dipped cap. Sprague 199D476X9020EE2
C11,C16,C33	4.7µF 16V tant. dipped cap. Sprague 199D475X9016BA1
C14,C21,C12	0.001µF 100V ±10% Sprague 1C10X5R102K100B
C13	0.022µF 50V ±20% Sprague 1C10Z5U223M050B
C17,C18	100pF 100V ±5% Sprague 1C10C0G101J050B
C23,C24	0.0022µF 100V C0G Sprague 1C10C0G222T050B
C25,C26,C27	.220µF 10V 20% solid tantalum KEMET T262D227M010MS or CSR21C227KM
C29,C30	0.0022µF 500V CER. DISK Sprague 5TSD22 or 5GAD22
CR1	Schottky diode T0-220AB DUAL Amperex BYV4335 or Motorola MBR2035CT
CR2	Zener diode 170V ±10% 5W IN5385A
CR3	UFRD 15 A 200 V T0 220 AC Single Amperex BYV29-200 or Motorola MUR1520
CR4	Zener diode 12V ±5% 1/4W IN4699
CR5,CR6	IN4001 1A 50V
CR7,CR8	UFRD AXIAL 1A 200V Amperex BYV27-200 or Motorola MUR120
CR9	IN4148 Signal diode
CR10,CR11	Schottky diode T0-220, DUAL Motorola MBR2545CT or Amperex BYV 43-45
Q1	MOSFET IRFP250 International Rectifier T0-247AC
Q2	TIP 29C TI bipolar transistor
Q3	MOSFET VP0104N3 Supertex or Plessy ZVP2106A
Q4	MOSFET VN1306N3 Supertex or Plessy ZVN3306A
R1	180 Ω 1/2W 5%
R2	3.9 kΩ 1/2W 5%
R3,R8	51 kΩ 1/4W 5%
R4	47 Ω 3W 5% RCD RSF2B or Clarostat VC-3D

Part No.	Description
R5	2.2 Ω 1/4W 5%
R6,R7	300 kΩ 1/4W 5%
R9	3.6 kΩ 1/4W 5%
R10	1 kΩ 1/4W 5%
R11	220 Ω 1/4W 5%
R12	36 Ω 1/4W 5%
R13	22 kΩ 1/4W 5%
R14	26.1 kΩ 1% 1/4W
R15	3.9 kΩ 5% 1/4W
R16	10 kΩ 1% 1/4W
R17	1 MΩ 5% 1/4W
R18,R22	470 Ω 5% 1/4W
R19,R20	1 kΩ 1% 1/4W
R21	10 kΩ 5% 1/4W
R23,R24	51 Ω 1W 5% RCD RSF1A
R25	100 Ω 5% 1/4W
L2	2µH ±5% Core: T68-2D Micrometals 10 Turns #30 AWG x 5 (wire length = 10 inches)
L3	MTI-125-02-02 GAP=.012 Multisource Technology Inductor
L4	330µH 0.6 ohm Inductor AL0410-331K Northeastern Electronics (315)455-7561
T1	Current Sense Transformer: Primary: 1 turn #18 AWG Secondary: 50 turns #34 AWG Core: Ferroxcube 1041CT060/3E2A
T2	MTT-125-DC-06-02-06C Multisource Technology Transformer
VR1	LM7812 12V regulator
U1	GP605 Gennum Resonant Mode Controller
U2	CNY17-4 TRW Opto-coupler
VR2	TL431 CLP TI Shunt Regulator
MOUNTING HARDWARE	4 - 40 nuts and flathead bolts TO - 220 insulating bushings Bergquist insulators K4 - 90, K4 - 35 Washers for PCB spacing Baseplate Heatsink PCB Keystone #8190 terminals with screws

REVISION DATE MAY 1990

GENNUM CORPORATION

The GP6040 in 50 W Series Resonant Mode Power Supply

APPLICATION NOTE

INTRODUCTION

In recent years, the state-of-the-art in practical power supply designs has been the Zero Current Switching, Quasi-Resonant converter, operating at higher and higher frequencies, in various topologies.

What is the reason behind this continuous trend towards high frequency? Is it only the human pursuit towards the unknown, or is it hard and cold cost calculation? It is hard to tell, given that power supply design is a constant trade-off between the quality of the electrical parameters, size, weight, efficiency and other regulatory aspects, such as limits on electromagnetic interference.

The Pulse Width Modulation technique, after 15 years of development, stretches up to 500 kHz to achieve ever smaller and more efficient converters. Recent developments in magnetic materials, as well as better and better high frequency capacitors, extend PWM's life to these extraordinary limits. However, despite all this advancement, this technology bears all the problems of early designs. The power switch has to commutate the inductor current at its peak. Due to high frequency operation, in pursuit of lower switching losses, the speed of the switches becomes higher and higher. This causes oscillation of the parasitic components, and thus causes EMI noise. Higher load in effect creates greater oscillation. Despite its constant frequency, PWM creates a wide spectrum of harmonics. Traditionally, this fact of life is solved with ever bigger filter components and in some cases, heavier outside shielding.

On the other hand, the Zero Current Switching technique (ZCS) offers the opportunity to overcome some of these problems. The switching losses are virtually nil, due to zero current transistor switching. The oscillation on the parasitic components is still present. However, because of the variable frequency operation, the EMI is low on light load (low repetition of the pulses), and on full load is not much higher due to the load damping effect.

The difficulty with design of the quasi-resonant converter resides in the number of available possibilities. The resonant technique offers a lot of advantages, allowing the basic topology to be customized for a given application. Quasi-resonant mode, for those who understand it, is becoming just another tool, similar to PWM, which in the early seventies found its place in a world dominated by linear power supplies. The main penalty of this topology is the level of complication, due to the behaviour of resonant circuits and the mutual interaction of the primary and secondary circuits. For this reason, it is advantageous, after preliminary analysis of the basic circuit, to simulate the topology on your favourite analog simulation software.

The goal of this design is to present the features of the GP6041 controller in a topology which has not been widely explored.

ELECTRICAL PARAMETERS

The purpose of this note is to provide another example of the simple design of a Zero Current Switching converter. Only the most important points of the design will be highlighted. A 50 W power supply is proposed with nominal input voltage 40 V (30V - 50V range) and output 12 V / 4.2 A. The efficiency target is 80%. The other parameters are user definable and are not important from the point of view of this application note.

CIRCUIT DESCRIPTION

The forward converter with resonant switch topology was chosen for this particular design (Fig.1). There are several reasons behind this decision. The forward PWM converter is quite well known, and some of the experience gained in PWM design can be applied.

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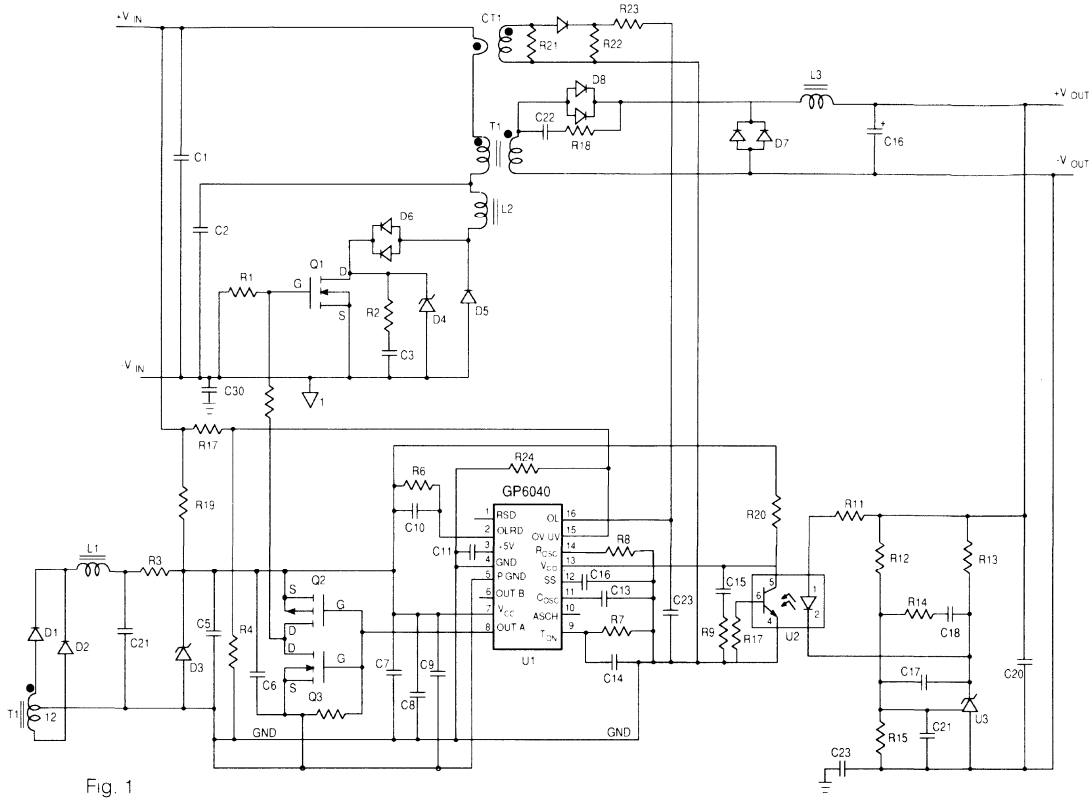

Fig. 1

The topology is simple and can be used for development of more complicated converters.

The calculations of the cicuit are conducted:

- all components are ideal with the exception of the transformer
- the circuit uses a diode to freewheel the output current
- the inductor is big enough, so the filter acts as the current source

DESIGN PROCEDURE

POWER TRANSFORMER PRELIMINARY CALCULATION

The power transformer is one of the main limiting factors of the modern power converter. It is not surprising that it is the first component to be specified. In recent months several ferrite core manufacturers have introduced new and very promising materials. The choice for this design is the high frequency material PC40 from TDK.

The variations of the flux density, due to square wave excitation cause two types of losses. Hysteresis losses

$$P_H = K_H \times f \times (B_{MAX})^Z \qquad (1)$$

are prevalent at low frequencies. The empirical equation (1) indicates that the hysteresis losses are linearly dependent on frequency. K_H is the hysteresis constant which depends on the high frequency material; Z is the Steinmetz constant which depends on the material and which varies between 1.6 and 2.

The eddy current losses are expressed empirically as

$$P_{ECL} = K_E \times f^2 \times (B_{MAX})^2 \qquad (2)$$

The value of the eddy losses are highly dependent on frequency. They dominate core losses at frequencies higher then 20 kHz. Despite the above equations the total core losses are often expressed by an empirical approximate formula:

$$P_{TCL} = (B)^X \times f^y \qquad (3)$$

For the ideal case X = 2 and y = 1. However the empirical approximation uses different exponent values. Empirically, for most magnetics materials, X = 2.4 and y = 1.3. The number of empirical constants in the above equations leads to the conclusion that the most reliable source of core loss calculation is the manufacturer s data sheets.

Let us assume that 400 mW core losses will be quite acceptable for a 60 W power transformer. In the first approximation the TDK core PQ 26/25 appears to be a reasonable size for a 50 W converter. The total effective value, from the TDK data sheet, is $V_E = 6.53\ cm^3$. For high frequency material H7F the losses of 400 mW for effective core value 6.53 cm^3 at frequency 600 kHz and temperature 100 °C requires a flux density no higher than $B_{MAX} = 58$ mT. To achieve full utilization of the topology, 90% maximum duty cycle is chosen. Therefore, the converter frequency is established as 540 kHz. This sets maximum flux density at $B_{MAX} = 65$ mT.

RESONANT TANK CALCULATION

The power stored in the resonant tank P_{RES} may be calculated by equation :

$$P_{RES} = \frac{L_R \times I^2_{R(pk)}}{2} \times f_{CONV} \qquad (4)$$

where L_R - resonant tank inductor
$I_{R(pk)}$ - resonant tank peak current
f_{CONV} - maximum frequency of the converter

To calculate resonant tank circulating current let use another equation:

$$I_{R(pk)} = \frac{V_{CR}}{Z_R} = \frac{V_{CR}}{L_R \times 2 \times \pi \times f_R} \qquad (5)$$

where L_R - resonant tank indicator
V_{CR} - voltage on resonant tank capacitor
Z_R - resonant impedance
f_R - the resonant frequency of the tank
than from (4)

$$L_R = \frac{2 \times P_{RES}}{I^2_{R(pk)} \times f_{CONV}} \qquad (6)$$

Solving (5) and (6) for $I_R(pk)$ gives

$$I_{R(pk)} = \frac{2 \times P_{RES} \times 2 \times \pi \times f_R}{V_{CR} \times f_{CONV}} \qquad (7)$$

The frequency of the converter and resonant frequency are determined during preliminary transformer design elaborations and chosen as 540 kHz and 600 kHz, respectivly. The maximum frequency will be applied to the circuit during the low input voltage $V_{IN} = 30$ V. The voltage on the resonant capacitor can, in the worst case, be doubled by the discharging action of the power transformer. Therefore

$$I_{R(pk)} = \frac{2 \times 50 \times 2 \times \pi \times 600{,}000}{60 \times 540{,}000} = 11.6\ A$$

This current represents the minimum resonant tank current at minimum input voltage. From this condition, it is possible to calculate resonant inductor and capacitor.
From (6)

$$L_R = \frac{2 \times 50}{11.6^2 \times 540{,}000} = 1.38\ \mu H$$

The C_R can be calculated from the equation:

$$C_R = \frac{1}{4 \times \pi^2 \times f_R^2 \times L_R} \qquad (8)$$

Than

$$C_R = \frac{1}{4 \times \pi^2 \times 600{,}000^2 \times 1.38 \times 10^{-6}} = 0.025\ \mu F$$

RESONANT TANK INDUCTOR CALCULATION

The number of the turns required to produce a 1.6 µH for the core T106-2 from Micrometals could be calculated from the trivial equation

$$N = 100 \sqrt{\frac{L}{A_l}} \qquad (9)$$

For $A_L = 135$ [µH/100 turns] number of the turns N = 10

Let us confirm that the maximum flux density does not exceed the design goal.
Faraday's law for sinewaves is described by

$$B = \frac{V_{RMS} \times 10^8}{4.44 \times f_R \times N_P \times A_E}\ Gauss \qquad (10)$$

where
B - peak AC flux density (Gauss) 1 Gauss = 10^{-4} Tesla
V_{RMS} - RMS voltage
N_P - number of turns on primary
A_E - effective core area

For $A_E = 0.69\ cm^2$ the peak flux density B = 173 Gauss. At frequency 600 kHz and 90% duty cycle, for core volume $V_E = 4.56\ cm^3$ from Micrometals data sheet, total core loses are $P_C = 779$ mW. If the input voltage is higher, the converter frequency is lower and core loses are lower, despite the higher RMS voltage.

FINAL TRANSFORMER CALCULATION

Traditionally the first parameter in transformer calculation is the turns ratio "N".

The turns ratio "N" is expressed as

$$N = \frac{V_{P(RMS)}}{V_O + V_D} \quad (11)$$

where

$V_{P(RMS)}$ - RMS voltage on the primary winding of the transformer
V_O - converter output voltage
V_D - voltage drop on the output diode

The peak primary voltage on the transformer in the worst case is $V_{P\,(pk)} = 1.5\ V_{IN\,(MIN)}$ and maximum voltage drop on the output diode is estimated at 1.5V.

The RMS primary voltage is calculated from equation

$$V_{P(RMS)} = V_{P(pk)}\sqrt{\frac{f_{CONV}}{4 \times f_R}} \quad (12)$$

Then for maximum converter frequency

$$N = \frac{28.4}{12 + 1.5} \approx 2$$

Now, one may determine the number of turns on the primary winding. Faraday's law for sinewave says that

$$B = \frac{V_{RMS} \times 10^8}{4.44 \times f_R \times N_P \times A_E} \quad \text{Gauss} \quad (13)$$

The magnetizing inductance

$$L_M = \frac{0.4 \times \pi \times N_P{}^2 \times \mu \times A_E \times 10^{-8}}{l_E} \quad (14)$$

where μ - material permeability
l_E - length of the flux path

The trapezoidal shape of the primary current waveform can be replaced with a square wave to simplify calculation (assuming that di/dt of the rising and falling edge of the current are equal). The $I_{P(RMS)}$ for a squarewave is described by equation

$$I_{P(RMS)} = I_{P(pk)}\sqrt{f_{CONV} \times t_{ET}} \quad (15)$$

The t_{ET} usually can be estimated by the equation

$$t_{ET} = 0.75\frac{1}{f_R} \quad (16)$$

Therefore with good accuracy the t_{ET} time is estimated as 1.25 µs.

To ensure zero current switching of the power transistor the resonant inductor current $I_{R(pk)}$ must be equal or greater than the peak primary current $I_{P(pk)}$. To allow for some parasitic

$$I_{R(pk)} = 1.2 \times I_{P(pk)} \quad (17)$$

Substituting $I_{R(pk)}$ from (8) and solving for $I_{R(pk)}$

$$I_{P(pk)} = \frac{V_{CR}}{1.2\sqrt{\frac{L_R}{C_R}}} \quad (18)$$

The worst condition is during low input voltage $V_{IN} = 30$ V and $V_{CR} = 60$ V

$$I_{P(pk)} = \frac{60}{1.2 \times \sqrt{\frac{1.38 \times 10^{-6}}{25 \times 10^{-5}}}} = 6.76\ A$$

The value of the RMS primary current can be calculated from the equation (15)

$$I_{P(RMS)} = 6.21\sqrt{540.000 \times 1.25 \times 10^{-6}} = 5.55\ A$$

Let us define the ratio M between the magnetizing current and the primary current as 1:3 to achieve best utilization of the core in a high frequency environment.

$$M = \frac{I_P}{I_M} = 3 \quad (19)$$

This kind of ratio (according to (20)) will result in total primary current only 5.7% higher than the reflected load current.

$$I_P = \sqrt{\frac{I^2_S}{N^2} + I^2_M} \quad (20)$$

The magnetizing current can be calculated from equation (19) giving $I_{M(RMS)} = 1.85$ A

The minimum magnetizing inductance L_M may be calculated by using equation

$$L_M = \frac{V_{P(RMS)}}{2 \times \pi \times f_R \times I_{M(RMS)}} \quad (21)$$

For $V_{P(RMS)} = 48$ V the calculated value of the magnetizing inductance is $L_M = 10.13$ µH.

Let us solve for N_P the equation (14)

$$N_P = \sqrt{\frac{L_M}{0.4 \times \pi \times \mu \times \frac{A_E}{l_E} \times 10^{-8}}} \quad (22)$$

Then for

$L_M = 12.4\ \mu H$

$\mu = 1500$

$A_E = 1.18\ cm^2$

$l_E = 5.55\ cm$

$$N_P = \sqrt{\frac{5.55 \times 10.13 \times 10^{-6}}{0.4 \times \pi \times 1500 \times 1.18 \times 10^{-6}}} = 1.55 \approx 2 \text{ turns}$$

Using equation (17) it is possible to verify if the calculated number of the primary turns meets the objective of not exceeding the flux density of $B_{MAX} = 65$ mT at the highest converter frequency $f_{CONV} = 540$ kHz. B = 66.8 mT. Calculated flux density slightly exceeds the design goal.

The turns ratio N = 2, was determined earlier and the number of the secondary windings is easily calculated as $N_S = 1$.

The winding losses are an important factor in transformer design procedure. There are new, advanced types of high frequency power transformers available (eg. planar transformers, matrix transformers). For this particular design, however, a more traditional method using the Litz wire will be used. At high frequency, the current conducted by the conductor, tends to be concentrated near the surface. The equation describing the skin depth of the copper conductor at room temperature is well known :

$$\delta = \frac{0.066}{\sqrt{f_R}} \qquad (23)$$

where δ is skin depth in meters.

In this design the resonant frequency is $f_R = 600$ kHz and the calculated skin depth is $\delta = 0.07$ mm = 2.76 mils. The #30 AWG wire is the perfect choice for the 600 kHz transformer. Total transformer power dissipation can be defined by the equation

$$P_T = P_{CORE} + P_{SEC} + P_{PRIMARY} = 410 + 254 + 320 = 974\ mW$$

POWER SEMICONDUCTORS

The topology used requires a bi-directional power switch. The most common solution is a MOSFET power transistor interconnected with two additional Schottky diodes (Fig 2).

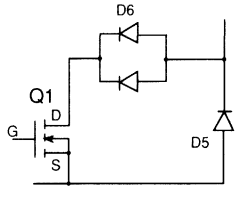

Fig. 2

The only purpose for D6 is to block an internal parasitic diode of the power MOSFET transistor. This internal diode is too slow to block high frequency current. The switch operates at maximum 90% duty cycle at minimum input voltage and nominal load. For this condition the converter operates at the maximum frequency set by the design, $f_{MAX} = 540$ kHz. The peak current commutated by MOSFET $I_{R(pk)} = 11.6$ A. The $I_{R(RMS)}$ can be calculated by the formula:

$$I_{R(RMS)} = I_{R(pk)} \sqrt{\frac{f_{CONV}}{4 \times f_R}} \qquad (24)$$

Therefore $I_{R(RMS)} = 5.5$ A

The power dissipation in the power transistor will be limited to conduction losses:

$$P_Q = I^2_{RMS} \times R_{DSON}\ (T_J = 100\ ^\circ C) \qquad (25)$$

For IRFP150 MOSFET(Q1); R_{DSON} $(T_J = 100\ ^\circ C) = 0.0675$

then $P_Q = 5.5^2 \times 0.0675 = 2.04$ W

The Schottky diode D6 in series with the power transistor conducts current identical to the one conducted by the MOSFET. Losses can be calculated from the following equation:

$$P_D = I_{RMS} \times V_{RMS}\ (T_J = 100\ ^\circ C) \qquad (26)$$

For MBR2035CT Schottky diode (D6), $V_{pk} \approx 0.6$ V.
$V_{RMS} \approx 0.268$ V, and $P_D = 1.474$ W.

The return diode D5 will conduct very little current at nominal load. Only at light load is significant current conducted but the duty cycle is very low. Although this diode must be rated for up to $I_{R(pk)}$ currents, it dissipates little power. This can be estimated to be about 0.25 W. The MUR1515 (D5) we chose has 150V reverse voltage and excellent 35 ns reverse recovery time.

Total Power Switch losses

$$P_{SW} = P_Q + P_{D1} + P_{D2} = 3.76\ W$$

DESIGNING THE GP6041 CONTROLLER IC INTO A POWER SUPPLY

A complete schematic diagram of the proposed converter is presented in Fig. 1.

1. Supply voltage and references

The layout of the power supply has to be very carefully analyzed. Great care must be taken to ensure that grounds are run so that any voltage drops from high ground currents are minimized and do not interfere with feedback voltages and references. To accomplish this task the converter provides two types of grounds, pin 4 - analog ground and pin 5 - power ground. Only the output transistor is connected to the power ground, to minimize interference with the logic circuity. GND and PGND are connected outside the package. The connection point is carefully chosen and decoupled by a 0.1 µF capacitor, C5. Pin 7, V_{CC} is decoupled to the PGND and GND pins almost directly on the IC by a 10 µF tantalum capacitor, C7, in parallel with 0.1 µF ceramic capacitors C8, C9. The +12 V voltage is chosen as an industry standard. The low startup current circuit allows the design of an inexpensive, energy efficient, power-up circuit. The resistor, R19, and zener diode, D3, dissipate only 0.25 W.

The +5 V voltage reference, pin 3, is used to power most of the internal circuity. This pin is decoupeld by a 2.2 µF tantalum capacitor, C11, in parallel with a 0.1 µF ceramic capacitor.

2. Power output

The choice between the GP6040 and the GP6041 controller is infact, the choice between direct drive of the power MOSFET and the use of some kind of predriver. The controllers are capable of delivering 200 mA of continous current to the resistive "load", at 70°C ambient temperature. In the case of this design, "the load" is IRFP251, the power MOSFET transistor. The input capacitance of this device is 2600 pF. The total power dissipation in the output stage of the converter can be calculated from the equation:

$$P = 2 \times \frac{C \times V_{CC}^2}{2} \times f_{CONV} \qquad (27)$$

where C is the total capacitance of the device, including the Miller capacitance. Let us estimate this total capacitance as three times higher than the input capacitance. Then the estimated total power dissipated in the output stage of the controller, is P = 786 mW. The plastic package of the GP6040 can dissipate a total of 720 mW at 70°C. From this calculation it becomes clear that it is necessary to use the predriver circuit to drive the power switch.

A totem pole small signal MOSFET stage, Q2 - Q3, is chosen as the most cost effective solution. It is possible to use any IC predriver available. In this case, the GP6040 output drives only about 70 pF load, and power dissipation of the output stage is limited to 21 mW. Both driver MOSFETs have R_{DSON} of 8Ω and can provide high current pulses to charge and discharge C_{GS} of the power MOSFET.

Since the GP6040 provides an active low, fixed pulse width output, it is perfectly suited for predriver configurations. For direct drive, the choice would be the GP6041 which provides an active high, fixed pulse width output. A small 0.1 µF capacitor, C6, decouples the Q2 - Q3 transistors.

3. Setting the oscillator parameters

Both controllers are capable of operating at the frequency f_{MAX} = 3 MHz. The oscillator capacitor C13 connected to the pin 11, controls the minimum frequency, f_{MIN} of the VCO operating range. This capacitor should be selected as the first component of the oscillator section. Fig. 5 from the Gennum data sheet No. 510-59 provides the proper value of the oscillator capacitor. A 220 pF ceramic capacitor with a temperature coefficient of -750 ppm/°C, is chosen. The resistor on pin 14 , R8 , controls f_{MAX}, the maximum frequency of the VCO operating range. Fig. 3 on the Gennum data sheet allows for selection of R8. f_{MAX} in this design is 540 kHz. The 15 kΩ, 1% resistor, with zero temperature coefficient, is chosen for good stability. Tolerance of f_{MAX} from chip-to-chip is ± 5% (456 kHz to 504 kHz).

The constant pulse width T_{ON} is set by parallel resistor R7 and capacitor C14, connected to the pin 9. This timing is used to shut off the power MOSFET, Q1, during return diode, D5, conduction. The best way to achieve it, is to terminate the T_{ON} pulse right in the middle of the negative half of the sinewave current:

$$T_{ON} = 0.75 \times \frac{1}{f_R} \qquad (28)$$

Then relative inaccuracy in T_{ON} will not affect circuit operation. The relationship between T_{ON} and the value of the external components is shown in Fig.1 for GP6040 and Fig. 2 for GP6041 on the 510-59 data sheet. The T_{ON} time is generated by a monostable multivibrator, and may have any required duration. The only limit is the minimum value of the resistor R13 ≥ 3.3 kΩ due to the current capability of the pin 9. The monostable works in retriggerable mode. It means that if the maximum frequency set by the external components is higher than specified in (29) the T_{ON} time remains constant, however the frequency will divide by two. For normal operation the maximum frequency should be set no higher than:

$$f_{MAX} \leq \frac{1}{T_{ON} + T_{DT}} \qquad (29)$$

where

T_{ON} - constant pulse width

T_{DT} - dead time specified in the Gennum data sheet.

If this requirement is not fulfilled, the controller divides the

output frequency by two.

In this case f_R = 600 kHz, and from (28), T_{ON} = 1.68 µs. To provide for 20% "dead-time", a 100 pF ceramic capacitor and 12.1 kΩ, 1% resistor are chosen for GP6040 (Fig. 2 of the data sheet 510-59).

4. Feedback loop

For this design a standard feedback circuit with shunt regulator is chosen. The TL431CLP shunt regulator with surrounding components produces the error signal transmitted via an optocoupler to the primary side of the converter. The proper level of the current in the photo transistor is set by an external resistor R20. For this design, an internal 10 kΩ (typ.) pull-up resistor, provided by the controller, is too big and an external resistor, R20 = 3 kΩ has to be used. In such a configuration, the VCO input (pin 13) is set at the level of 4 volts, in the middle of the 1.5 V - 6.5 V range of the VCO. The control characteristic of the VCO input is shown in Fig. 4 of the Gennum data sheet. For this design and a variety of others, it is advantageous to have the direct access to the VCO input (no error amplifier). This allows the use of application-oriented devices to obtain an error signal while maintaining the reasonable price of the controller. However, if for some reason it is necessary to have an error amplifier built into the controller, please contact Gennum for price and delivery.

5. Startup block

To provide a slow initial charge of the output capacitors and prevent voltage spikes on the active components due to excessive current, the GP6040 controller provides a relatively slow change in the VCO operating frequency from minimum value, (about 8 kHz for C_{OSC} = 220 pF) to the one which is set by the feedback loop. The result is soft startup of the power supply. The rate of the change is controlled by a capacitor C_{SS} on this pin 12. The delay is approximately

$$T_{SS} = 0.6 \times R_{SS} \times C_{SS} \qquad (30)$$

where

C_{SS} - soft-start capacitor

R_{SS} - external resistor (if resistor not used R ≈ 5.1 MΩ, 20%)

In this case, the accuracy is not important; the goal is to use the smallest possible capacitor, therefore an external resistor is not used. For 20 ms startup time, the calculated capacitor C12 = C_{SS} ≈ 6.8 nF.

6. Overload Protection

Two pins are provided to deal with the overload conditions. A voltage exceeding the specified threshold on pin 16, will cause the GP6040 to synchronously shutdown and activate the overload restart delay function. Input on pin 2 sets overload restart delay. Timing starts when the overload is removed; upon time-out soft-start begins. As in the majority of power supplies, the current sensing is provided by a current transformer CT1. Its 1:20 turns ratio reduces the primary current of the power transformer , T1, by a factor of 20. The resulting voltage drop across the sensing resistor, R21, is applied to pin 16 of GP6040 via resistor capacitor filter R23, C23. The time constant of this filter is 5.3 µF. Therefore the voltage across C23 looks like a sawtooth. Once the level reaches 3.2 V (±0.3 V), the controller shuts down the power converter for a period of time set by capacitor C10. From Fig. 6 on the Gennum data sheet, for R6 = 300 kΩ and C10 = 6.8 µF, this overload restart delay is about 0.7 seconds. If the overload condition remains (a possible short on the output), the power converter will continue to try to come back on-line with 20 ms soft-start every 0.7 sec. The resulting average current into the short will be very low, less than 0.05 I_O.

7. Shutdown section

Pin 15 is used to prevent the converter from operating in undervoltage or overvoltage input line condition. This input is a window comparator. A higher or lower voltage than the threshold specified will synchronously shutdown the power supply until the input voltage falls within the window again, at which point the GP6040 goes into soft-start. The minimum input voltage is U_{MIN} = 30 V and U_{MAX} = 50 V. To maintain 10% safety margin those voltages translate to U_{MIN} = 27 V and U_{MAX} = 55 V. The pin description in the 510-59 data sheet outlines in detail the steps to calculate the necessary components. From there, R17 = 10 kΩ, R4 = 560 Ω, R24 = 3.59 kΩ. Two remaining shutdown inputs, pin 1 and pin 10, have some different capabilities. Pin 1 is not used in this design and should be left floating. Pin 10 however, has very special features and could be used in the application as presented below in this Fig. 3.

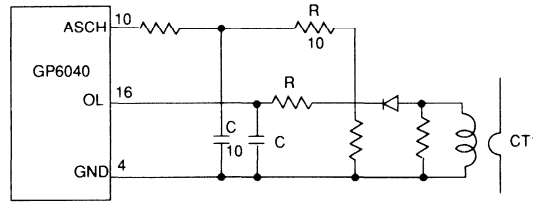

Fig. 3

If the current in the primary power circuit exceeds 10% of the preset maximum current on the overload shutdown input, the controller shuts down the converter permanently in asynchronous mode. Such operation may prevent transistor damage in some catastrophic failures (eg. shorted output diode). There are two ways to reset the asynchronous shutdown. By disconnecting the V_{CC} line, or by forcing pin 10 to a level below 0.5 V (typ).

OUTPUT SCHOTTKY

Switching losses are low due to the slow di/dt of the current.

$$P = 4.2\ A \times 0.55\ V = 2.3\ \text{watts}.$$

SNUBBERS

The circuit includes two snubber circuits. On the primary side the snubber is attached to the power transistor, and on the secondary, the snubber is across the rectifier. The power losses can be calculated as follow:

$$P = \frac{C \times V^2}{2} \times f_{MAX} \qquad (31)$$

For C3 = 470 pF, V = 100 V and C22 = 2.2 nF, V = 15 V for converter frequency f_{MAX} = 540 kHz the total losses are P = 1.4 W + 0.13 W = 1.15 W.

POWER SUPPLY EFFICIENCY

Power switch loss	3.76	W
Output Schottky diodes losses	2.2	W
Losses in snubbers	1.4	W
Power transformer losses (est)	0.98	W
Control/drive circuit	0.6	W
Output inductor dissipate (est)	1.0	W
Resonant tank dissipation	0.9	W
TOTAL LOSSES	10.84	W

Estimated efficiency

$$= \frac{50\ W}{60.84\ W} \times 100\ \% = 82.2\%$$

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REVISION DATE JUNE 1990

GENNUM CORPORATION

Retrofitting the GP6040/1 into a GP605 Circuit

INFORMATION NOTE

INTRODUCTION

The high performance GP6040 and GP6041 resonant mode controllers provide some additional features as compared with their predecessor GP605.

This information note provides easy to implement steps to retrofit the high performance GP6040/1 controllers into the single-ended topologies where the GP605 controller was previously used.

The following pin description outlines all differences between these IC's.

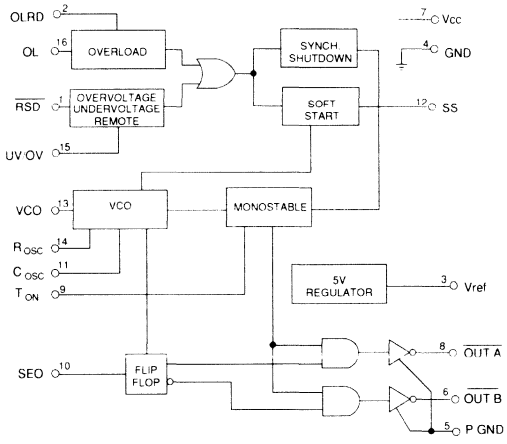

Fig 1. Functional block diagram of the GP605 controller

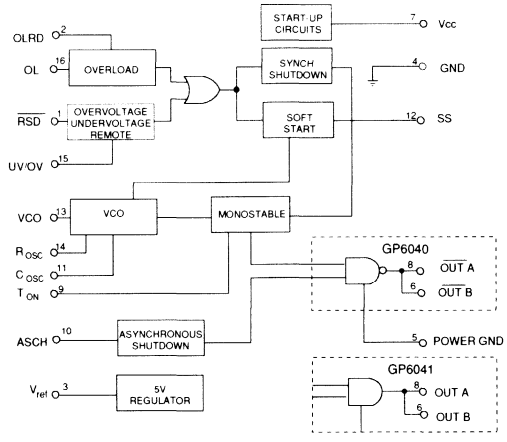

Fig 2. Functional block diagram of the GP6040/1 controller

GP6040/1 PIN FUNCTIONS

(Differences to compare with GP605)

Pin 1 (RSD) – Remote Shutdown
No difference in the parameter values or functions.

Pin 2 (OLRD) – Overload Restart Delay
No difference in the parameter values or functions.

Pin 3 (V_{REF}) +5V Reference
No difference in the parameter values or functions.

Pin 4 (GND) – Ground
No difference in the parameter values or functions.

Pin 5 (PGND) – Power Ground
No difference in the parameter values or functions.

Pin 6 (OUT B) – Output B
No difference in the pin function.

The GP6040 and GP6041 are single-ended devices. They provide, respectively, an active low or active high fixed pulse width output (Eg. on GP6041 - active high means that during start-up and shutdown conditions the controller introduces a low level on the output. High level output is only during the fixed pulse time period).

Pin 7 (V_{CC}) – Supply Voltage
The controller is equipped with a low start-up current circuit. The hysteresis is adjusted as follows: turn on at 13.0 V (typ) and synchronous turn-off if the voltage drops below 9.0 V (typ). If different threshold voltages are required, please contact Gennum's Power Department.

Pin 8 (OUT A) – Output A
No difference in the pin function.

This output has all basic characteristics identical to the Output B (pin 6) but is connected to it through a 1.5Ω ± 20% serial resistor. If this output is used power dissipation of the resistor should be included in the calculation of the total power dissipation of the controller.

Pin 9 (T_{ON}) – Pulse Width
No difference in the pin function.

The constant pulse width T_{ON} is set by resistor R_T and capacitor C_T. The values of the resistor and capacitor used in the GP6040/1 differs from those used in GP605 for the same pulse width T_{ON}.

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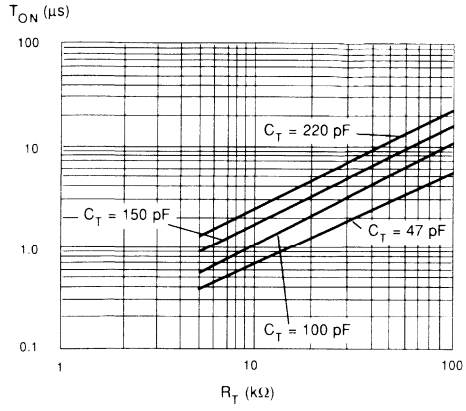

Fig 3. GP605 Output Pulse Width

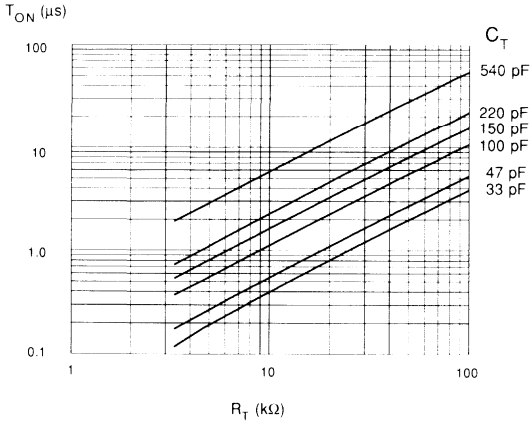

Fig 4. GP6040 Output Pulse Width

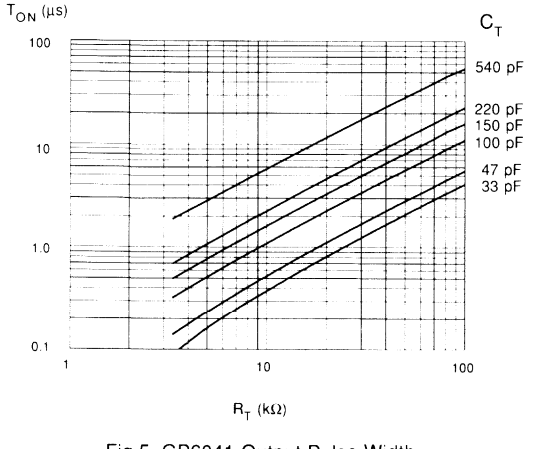

Fig 5. GP6041 Output Pulse Width

Pin 10 (ASCH) – Asynchronous Shutdown

In the GP605 this input is used to determine if the controller is performing single-ended or complementary operation. In the GP6040 and GP6041 this function is not necessary since these devices are designed specifically for single-ended operation.

Instead, this pin is used to accomodate the additional feature of asynchronous shutdown.

The asynchronous shutdown means that the controller jumps to standby mode immediately (70 ns typ.) after the high level on pin 10 is detected. All other inputs feature synchronous shutdown wich allow active constant pulse to end despite the fact that the shutdown function is activated.

In zero current switching topology, ASCH may prevent transistor damage during some catastrophic failures (eg. short Output diode). The triggering level of the asynchronous shutdown is set in such way that it is possible to use it simultaneously with the overload sense circuit.

In ZCS topology ASCH input is meant to be used in emergency situations only. Asynchronous shutdown is also necessary to support zero voltage switching operation.

For detailed pin description refer to GP6040/1 data sheet, document 510-59.

Pin 11 (C_{OSC}) – Oscillator Capacitor

No difference in the pin function.

The capacitor on this pin, C_O, controls the minimum frequency f_{MIN} of the VCO operating range. The value of the capacitor used in the GP6040/1 to obtain the same minimum frequency differs slightly from that used in the GP605.

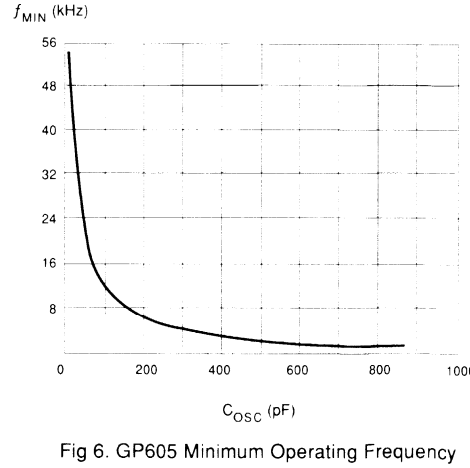

Fig 6. GP605 Minimum Operating Frequency

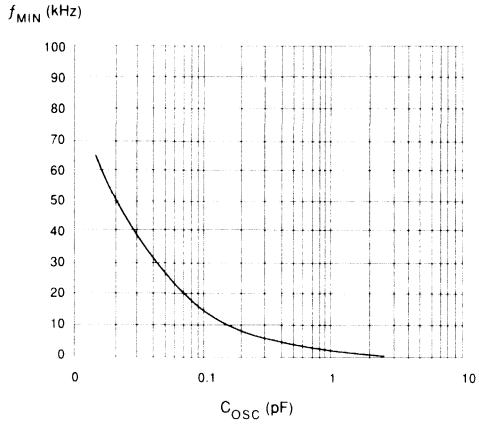

Fig 7. GP6040/1 Minimum Operating Frequency

Pin 12 (SS) – Soft-start
No difference in the pin function.

A capacitor C_{SS} on this pin provides a controlled start-up from f_{MIN} to the frequency set by the VCO Input. The delay is approximately

$$t_{SS} \approx 0.6 \times R_{SS} \times C_{SS}$$

where

C_{SS} - soft-start capacitor
R_{SS} - external resistor
(if resistor not used R = 5.1 MΩ ± 60%)

The GP605 has an internal 10 kΩ pull-up resistor. In the GP6040 and GP6041 this resistor has been removed and replaced with a very low value current source. For this reason the value of the capacitor is much smaller than the one used with the GP605. The accuracy of the soft-start due to low accuracy of the current source, is very low. If high accuracy of soft-start is necessary, attach a 10 kΩ pull-up resistor. In such a configuration the value of the capacitor is the same as that in the GP605 to obtain a comparable soft-start frequency rise.

Pin 13 (VCO) – Voltage Controlled Oscillator Input
No difference in the pin function.

The oscillator can function up to 3 MHz on higher duty cycle as compared with 2 MHz for the GP605.

Pin 14 (R_{osc}) – Oscillator Resistor
No difference in the pin function.

The resistor on this pin, R_O, controls f_{MAX}, the maximum frequency of the VCO operating range. The value of the resistor used in the GP6040/1 to obtain the same maximum frequency differs slightly from that used in GP605.

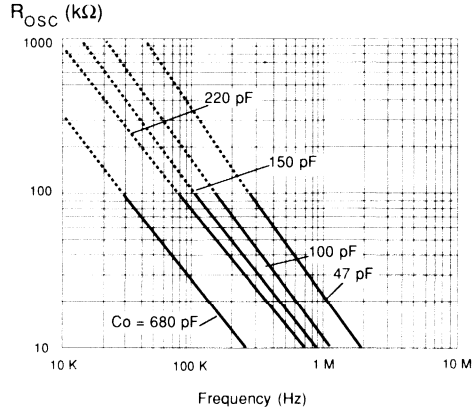

Fig 8. GP605 Maximum Operating Frequency

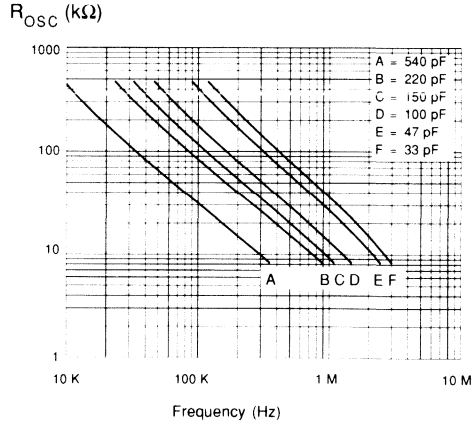

Fig 9. GP6040/1 Maximum Operating Frequency

Pin 15 (UVOV) – Undervoltage/Overvoltage Shutdown
No difference in the pin function.
The overvoltage level is adjusted as compared with the GP605.

Pin 16 (OL) – Overload Input
No difference in the pin function.
The overcurrent level is adjusted as compared with the GP605.

X486 Evaluation PC Board Assembly Manual

INFORMATION NOTE

INTRODUCTION

The GP6040 (active low output) and GP6041 (active high output) are simple yet versatile IC's allowing the designer to accomplish control functions with a minimum number of components. For proper operation, the GP6040/1 requires only four essential elements: R_O, C_O (VCO timing components), R_T and C_T (pulse width setting components). All other elements perform either filtering or "housekeeping" functions.

The X486 evaluation board can be used in two ways. One third of the board contains space for all the components necessary to build an open loop test circuit and evaluate the GP6040/1. The remaining part of the board allows the designer to build various types of Resonant Mode Converters. The first step to familiarize oneself with the controller is to read the functional pin description published in the GP6040/1 data sheet.

OPEN LOOP TEST CIRCUIT

To assemble the open loop test circuit use schematic diagram (Fig.5) and the open loop test circuit components layout (Fig.6). The recommended parts are listed in the bill of material. It is recommended to assemble the board step by step following comments in this manual.

The components called "essential" should have leads as short as possible. Note that all "essential" and "house keeping" components are connected to the analog ground. To evaluate parameters of the controller, running close to the maximum frequency 3 MHz, it may be necessary to replace the potentiometers with high frequency resistors. The ground layout and the place of the interconnection between analog and power grounds is particulary important to proper operation of the controller. Improper ground connection can create various noise problems. The power and analog ground are to be connected on the PC-board by the jumper J1. Such an arrangement allows experiments with different ground configurations.

OSCILLATOR SECTION

Assemble the following components which are essential to proper operation of the controller.

The oscillator capacitor C_O (C11) connected to pin 11 controls minimum frequency. This capacitor must be selected as a first component of a control circuit.

The equation to calculate f_{MIN} is very complicated thus the data sheet provides the relationship between minimum VCO frequency and capacitor value. Layout is critical for this component and leads should be as short as possible.

The oscillator resistor R_O (assemble serial connection of R6 and P1) connected to pin 14 controls maximum frequency of the VCO operating range. The value of the resistor, for a given value of the oscillator capacitor, can easily be read off the graph presented in the data sheet. The minimum value of the oscillator resistor is 8.2 kΩ. The smaller the resistance the wider the frequency range.

The RC network connected to pin 9 consists of resistor R_T (assemble serial connection of R11 and P2) and capacitor C_T (C12). The value of both components can be obtained from the graph published in the data sheet. The minimum value of the resistor R_T is 3.3 kΩ.

The components recommended in the bill of material allow one to vary the frequency from 13.3 kHz to 1.2 MHz. To operate in the 3 MHz region replace the resistor R6 and potentiometer P1 with a single high frequency resistor R6 as well as the resistor R11 and potentiometer P2 with a single high frequency resistor R11 (Fig.1).

To allow the controller to oscillate freely, it is necessary to assemble some of the non-critical components to provide certain voltage levels on the housekeeping input pins.

Apply 2.5 V on pin 15 (undervoltage/overvoltage shutdown). To achieve this, connect resistors R8, R9 and a four section dip switch SW1. Set switch S3 to ON position.

Apply 2.5 V on pin 16 (overload shut down). Set S4 to ON position and connect resistors R7, R10.

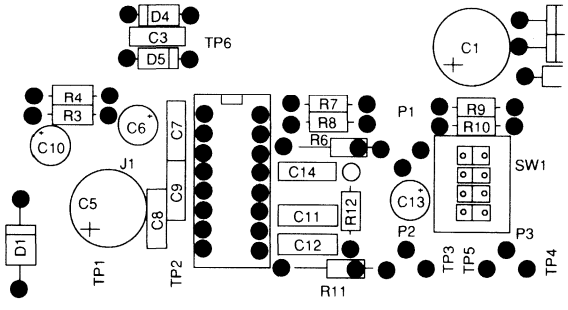

Figure 1 (Actual Size)

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To avoid a shut down condition, set switches S1, S2 to OFF positions.

The voltage on VCO can be obtained in two ways: by connecting a voltage source to TP3 (V_{VCO}) and TP4 (GND) or, if additional voltage source is not available, by applying a jumper between TP3 - TP5 and assembling a potentiometer P3.

The potentiometer when connected to the 10 k Ω internal pull-up resistor allows one to vary VCO input voltage. The linear input range is from 1.1 V to 6.5 V but the maximum voltage on VCO is V_{CC}.

Set VCO input voltage to maximum value (6.5V) or, if using the potentiometer, adjust P3 to the maximum counter clockwise position.

Set the potentiometers P1 and P2 to maximum counter clockwise position.

Set the oscilloscope to 1 µs/div and 5 V/div.

Connect together power and analog grounds (jumper J1).

Install V_{CC} filter capacitors C5, C9, C8 and, most importantly, V_{REF} decoupling capacitors C7 and C6.

Assemble bias resistors R3 and R4. The role of those components in the circuit is described in overload - shutdown section.

If for any reason the voltage on the output pins goes below GND level or above V_{CC} by more than 0.5 V assemble diodes D4 and D5. For open loop test circuit purposes diode D5 could be replaced by the load resistor.

POWERING UP GP6040/1

Connect the voltage source to TP1(V_{CC}) and TP2 (GND).

Raise the voltage from 0 V to 13 V. At 11.5 V (typ.) the controller V_{CC} undervoltage function allows the VCO to oscillate.

On pins 6 and 8 identical trains of pulses should immediately appear (Fig.2).

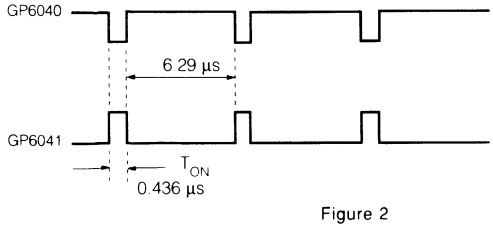

Figure 2

When V_{CC} is reduced to 8.5 V (typ.) the V_{CC} undervoltage function is activated again and synchronously shuts down the oscillation. The V_{CC} hysteresis is typically 30%.

Set T_{ON} time to 6 µs by slow adjustment of the potentiometer P2.

Observe frequency change with constant T_{ON} time when varying the VCO input voltage from 0 V to V_{CC} (try full range of the potentiometer P3).

Adjust VCO voltage (P3) to obtain frequency 100 kHz (full period T_{OSC} = 10 µs).

Reset frequency to 200 kHz (full period T_{OSC} = 5 µs) by slow adjustment of the potentiometer P1 (R_O).

At this point, if you try to increase the frequency to 250 kHz (T_{OSC} = 4 µs) by varying VCO voltage (P3), the frequency will divide itself by a factor of two. Note that the frequency of the oscillator (pin 11) did nor change. The division means that two consecutive ON pulses were closer than 80 ns / 100 ns (typ) (GP6040/1 deadtime).

This option could be used as an inherent current limit for some topologies.

If frequency division is not required it is enough to properly choose R_O (R_O sets maximum frequency).

Note that the setup of the maximum frequency of the controller and correct choice of the T_{ON} time in effect determines the dead time (minimum dead time is 80 ns/ 100 ns).

To obtain soft start capabilities install capacitor C13. Now, if supply is applied, the frequency does not jump instantly but rises from minimum to level set by VCO input. The charge for the soft start capacitor is provided by the transistor base bleed current. If there is a requirement for a faster frequency increase (startup) install resistor R12.

SHUTDOWN SECTION

If you have a digital storage oscilloscope you may wish to experiment with the GP6040/1's extensive shutdown capabilities.

Undervoltage / Overvoltage Synchronous Shutdown (pin 15) - By switching S3 ON and OFF you can observe the synchronous shutdown on the outputs (pins 6 and 8).

Synchronous shutdown is defined as the ability to allow the ON pulse to finish. This kind of shutdown is meant to be used with standard power supply turnoffs. When UV/OV pin is released, the controller performs the normal soft start function, Fig. 3.

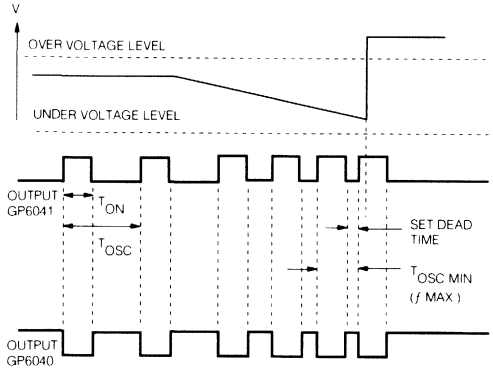

Figure 3

To change overvoltage and undervoltage threshold levels from those preset internally, apply resistor between UV/OV input (pin 15) and reference voltage (pin 3) Fig. 4.

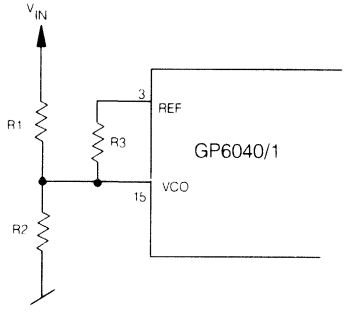

Figure 4

The value of the resistors can be calculated from the following equations:

$$R3 = \frac{(V_o \times V_r) - (V_u \times V_r)}{(V_u \times V_{ino}) - (V_o \times V_{inu})} \times R1$$

$$R2 = \frac{R1 \times V_r \times (V_o - V_u)}{V_r \times (V_{ino} - V_{inu} + V_u - V_o) + (V_o \times V_{inu} - V_u \times V_{ino})}$$

where

V_o - the GP6040/1 overvoltage threshold lockout
V_u - the GP6040/1 undervoltage threshold lockout
V_r - required voltage - 5V
V_{ino} - required line overvoltage lockout
V_{inu} - required line undervoltage lockout

Overload Synchronous Shutdown (Pin 16) – This overcurrent protection is meant to be used with a current transformer. For a demonstration of the function, turn the switch S4 ON and OFF. You can observe on the output the synchronous shutdown function as described in the UV/OV (pin 15) paragraph. Install C10. Those components connected to pin 2 introduce delay to the soft start function. Now if switch S3 is turned ON , the controller start up function is delayed for the time determined by the RC network. In this way, it is possible to set maximum average current in an overload condition.

Remote Synchronous Shutdown – This function is identical to UV/OV shutdown and the only difference is the input trigger voltage level. To experiment, use switch S1.

Asynchronous Shutdown – This option is designed to provide immediate (80ns / 60ns GP6040/1 typ. delay) termination of the pulses. This is necessary in some designs to prevent serious damage (eg. fire) under fault (eg. short output diode) conditions. To reset asynchronous shutdown force pin 10 to the level lower than 0.5 V. Experiment with this feature by use of the switch S2. If the evaluation board you received does not have revision level printed on the PC board, the additional resistor R14 needs to be connected as per schematic diagram on Fig. 5.

PLEASE EXPERIMENT AND FAMILIARIZE YOURSELF WITH OUR SINGLE ENDED CONTROLLERS GP6040 OR GP6041. IF AT THIS POINT YOU HAVE ANY QUESTIONS CONTACT GENNUM CORPORATION DIRECTLY BY TELEPHONE OR FAX.

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DEVELOPMENT BOARD

As mentioned above, the X486 PC board can be used as a development board for experimental resonant mode power supplies. Fig.7 outlines areas reserved for input filters, power transistors, transformer, feedback circuit, inductor, output filters and additional power and logic components. This size of board is adequate for an experimental power supply in resonant mode topologies of up to 150W.

To support your design effort, Gennum Corporation publishes two application notes describing Half Bridge and Forward Mode Zero Current Switching Topologies. Gennum is now preparing new application notes based on the X486 development board.

X486 EVALUATION KIT

U	GP6040 and GP6041 Gennum Corporation Resonant Mode Controller
PCB	Evaluation / Development PC Board

RECOMMENDED BILL OF MATERIAL

PART No.	DESCRIPTION	
C1,C5	47 µF 20V tantalum dipped capacitor	Sprague 199D476X9020EE2
C2, C13	0.22 µF 50V Z5U +/ -20%	Sprague 1C10Z5U224M050B
C3,C4,	100 pF 100V +/ -5%	Sprague 1C10C0G101J050B
C6,C10	4.7 µF 16V tnatalum dipped capacitor	Sprague 199D475X9016BA1
C7,C8,C9	0.1 µF 50V Z5U +/ -20%	Sprague 1C10Z5U104M050B
R1,R2	100 kΩ 1/4W 5%	
R3,R4	300 kΩ 1/4W 5%	
R13, R6, R14	10 kΩ 1/4W 5%	
R7,R8,	4.7 kΩ 1/4W 5%	
R9, R10,R11	3.9kΩ 1/4W 5%	
P1,P2	100 kΩ potentiometer	Bourns 3329P-1-104
P3	25 kΩ potentiometer	Bourns 3329P-1-253
D1,D2,D3	1A 200V	Amperex BYV27-200 or Motorola MUR120
L1	330 µH 0.6 kΩ inductor	AL0410-331K Northeastern
VR1	12V regulator	Motorola MC78M12CT
SW1	Four section DIP switch	Grayhill 78B04

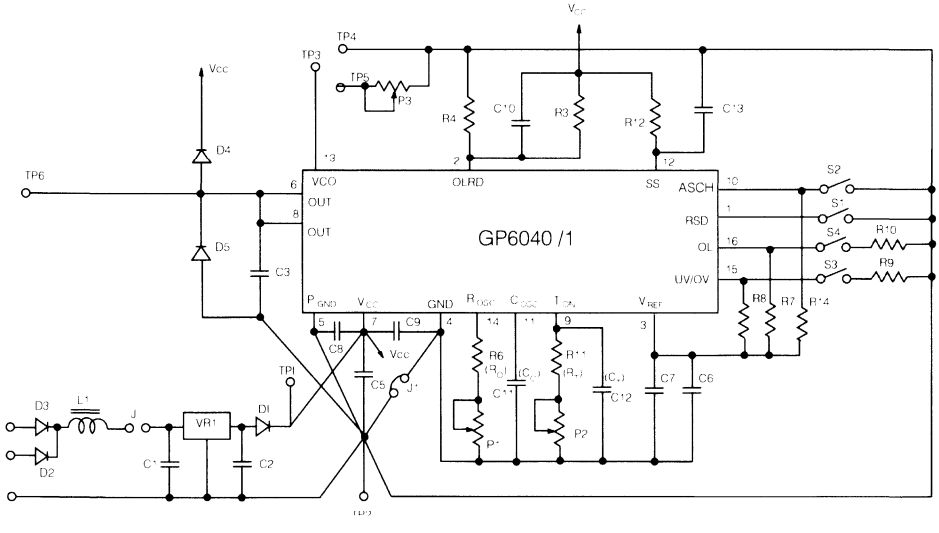


Figure 5

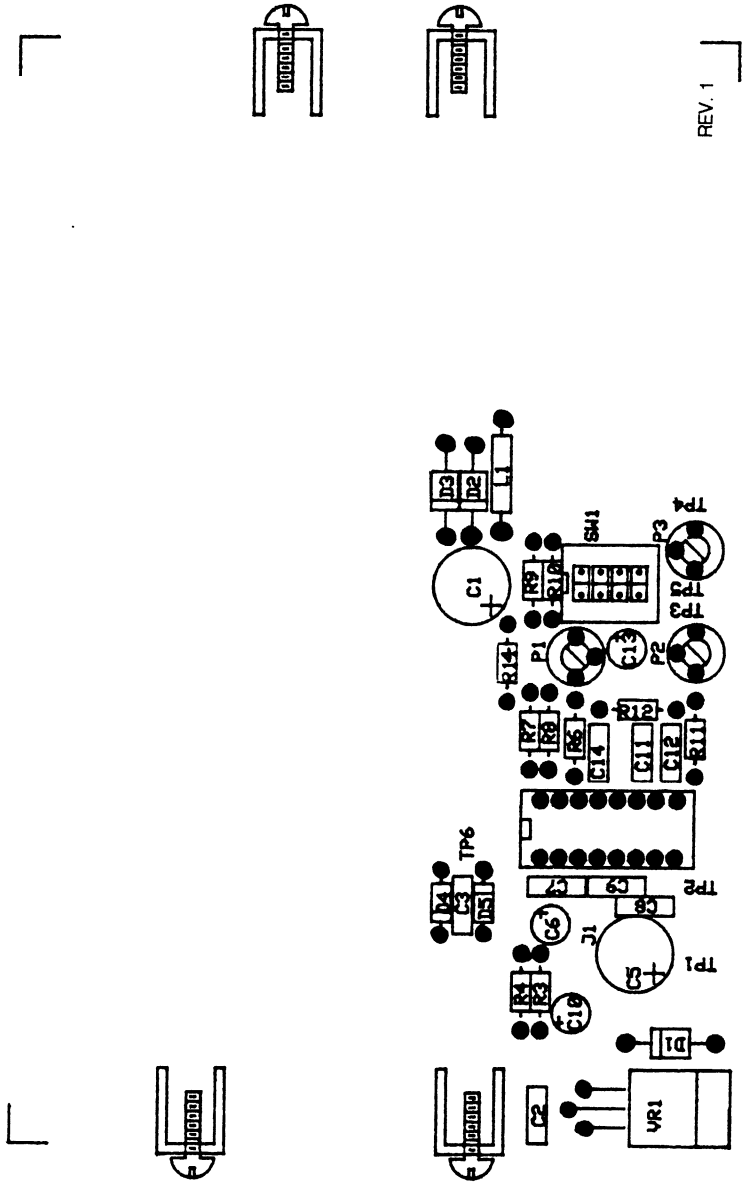

REV. 1
L1
D3
D2
C1
SW1
TP4
P3
TP3
R9
R10
P1
C13
P2
R14
R12
R7
R8
R6
C14
C11
C12
R11
TP6
D4
C3
D5
C5
J1
TP2
C8
TP1
R4
R3
C10
D1
C2
VR1

Figure 6

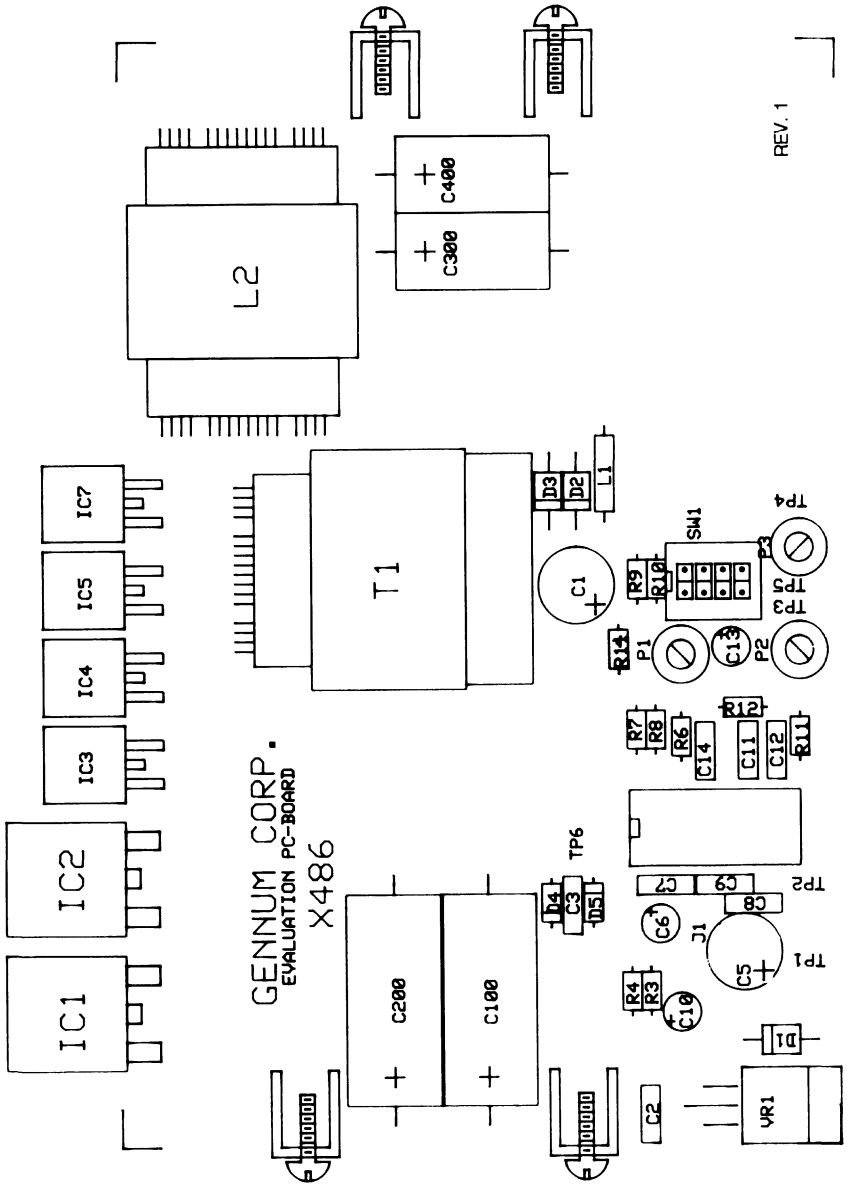

GENNUM CORP.
EVALUATION PC-BOARD
X486
REV. 1
L2
C400
C300
T1
D3
D2
L1
C1
SW1
TP4
TP3
P3
R9
R10
P1
P2
C13
R14
R7
R8
R6
C14
C11
R12
C12
R11
TP6
D4
C3
D5
C200
C100
C7
C9
C8
TP2
C6
J1
C5
TP1
R4
R3
C10
D1
C2
VR1
IC1
IC2
IC3
IC4
IC5
IC7

Figure 7

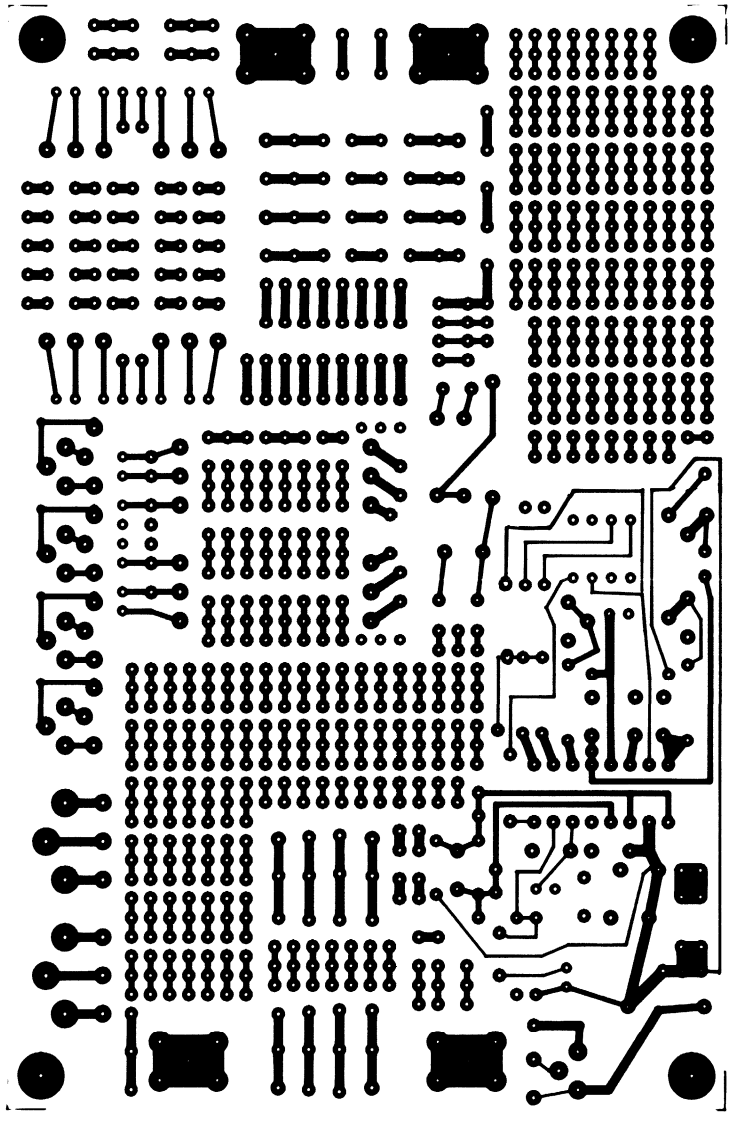


Figure 8
SOLDERING SIDE

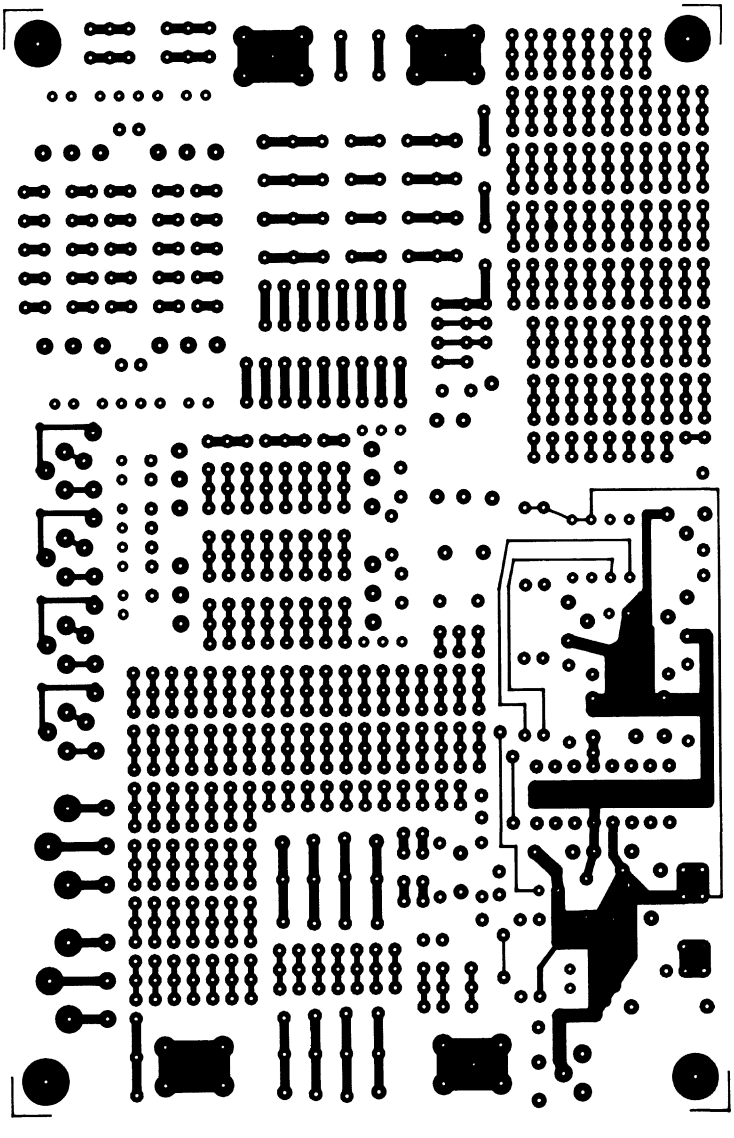


Figure 9
COMPONENTS SIDE

GENNUM CORPORATION

DC-DC Converter Kit - X485

INFORMATION NOTE

FEATURES

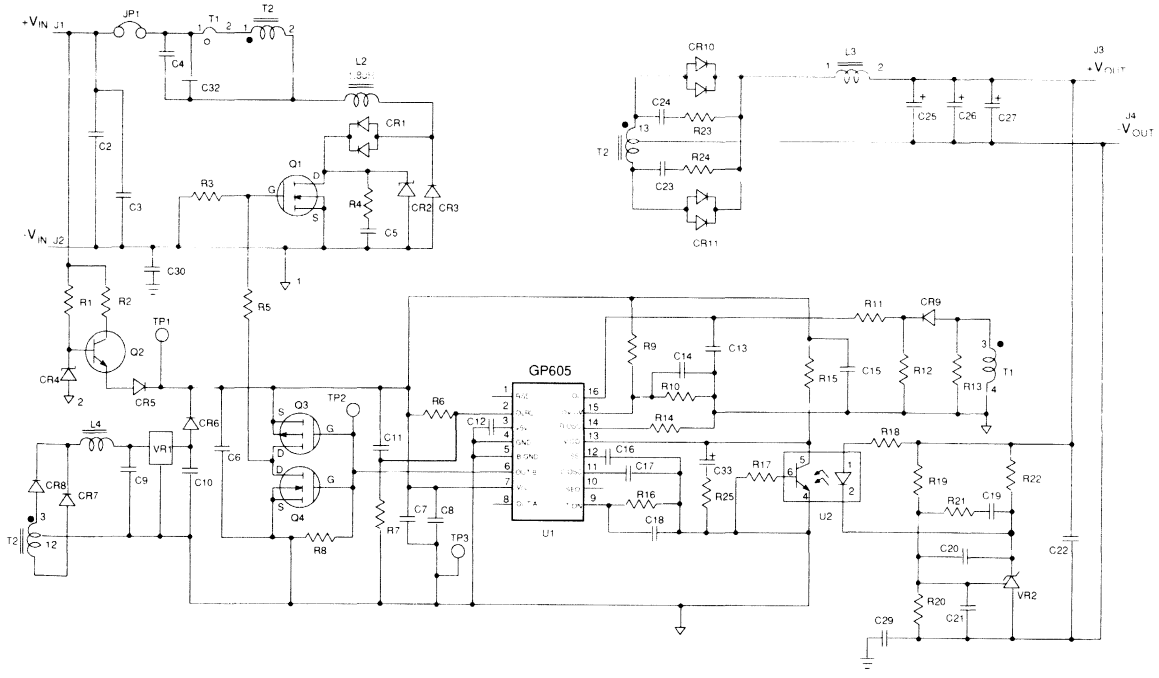
- small size 5.25" x 3.5" x 0.625"
- high power density
- lightweight
- small inductors and transformers
- 500 kHz switching frequency
- 100 W 5V output
- high efficiency 82%
- ideal for onboard power supply applications
- wide input range 36 V - 60 V DC
- overload protection
- short circuit protection

48V Input to 5V at 20 A Output, DC-DC Converter using the GP605 Resonant Mode Controller IC

This is a power supply kit being offered to demonstrate the potential of resonant mode as a control method for high performance power supplies.

The topology is based on a single-ended forward converter that has been converted to zero current switching by the introduction of a series resonant LC tank.

The GP605 resonant mode controller is a dedicated high performance controller that is used in this design. The GP605 provides the gate drive signal to the switching MOSFET. The GP605 generates fixed pulses at a varying frequency to regulate the output voltage. As well as providing the control, the GP605 also provides all the necessary peripheral functions such as Softstart, Undervoltage, Overvoltage and Overload Shutdown.



DC - DC Schematic

GENNUM CORPORATION P.O. Box 489, Stn A, Burlington, Ontario, Canada L7R 3Y3 tel. (416) 632-2996 fax: (416) 632-2055 telex: 061-8525
Japan Branch: 301 Aoba Building, 3-6-2, Minato-ku, Tokyo 108, Japan tel. (03) 441-2096 fax: (03) 448-8991

DC-DC Converter Kit

Specifications

Size 5.25" x 3.5" x 0.625"

Input voltage 36 VDC - 60 VDC

Output 5VDC at 20A

Efficiency 80%

Line Regulation ±0.1%

Load Regulation ±0.5%

Output Ripple 50 mVpp

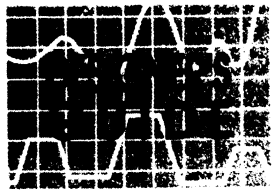
Kit Components

To eliminate any problems associated with resonant mode evaluation, the DC-DC Converter Kit is a complete power supply provided in unassembled form. The kit is comprised of all necessary components including the PCB, heatsink, and backplate.

To simplify the assembly and testing, a manual is also provided showing how to assemble the power supply, and how to test for proper operation. All the major waveforms are provided for comparison.

For information on the theory and development of an original design ask for the Gennum Application Note 510-63, *The GP605 in Variable Frequency Zero Current Switching, Forward Mode, Resonant Power Supply*.

Document No. 600-13



Resonant-Mode
Power Supplies

Resonant-mode design techniques improve switcher performance

3-77

Frederick E Sykes, *Gennum Corporation*

P.O. Box 489, Station A, Burlington, Ontario, Canada L7R 3Y3
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Resonant-mode design techniques are becoming increasingly attractive to power-supply designers because they lead to fewer switching losses and allow you to use smaller components. Part 1 of this 2-part article reviews the classifications and circuits of the various resonant-mode topologies. Then, a 5V-power-supply design example illustrates the waveforms and control requirements of a typical resonant-mode design. Part 2 will detail the design of the control loop, resonant tank, and transformer.

Part 1

One of the advantages of resonant-mode power supplies is that they can operate at higher switching frequencies than PWM designs, allowing you to use smaller transformer and output-filter components. In addition, resonant mode's use of sine-wave current and voltages reduces switching losses, EMI, and component stresses. Further, the availability of dedicated, resonant-mode control ICs makes it easier to implement a resonant-mode design.

This article discusses the most common types of resonant-mode supplies, which contain the central components of PWM designs along with two additional components: a resonant inductor and resonant capacitor (**Fig 1**). Recently, these types of resonant-mode converters have been called "quasiresonant." The resonant-mode technique uses this inductor and capacitor, which comprise a resonant tank, to achieve lossless switching by shaping the transformer's voltage and current. In PWM designs, the power switches are directly tied to their transformers, but in resonant-mode designs, the resonant tank sinusoidally shapes the transformer's input signal.

Another difference between PWM and resonant mode is in the regulation method. PWM designs regulate their outputs by fixing the control frequency and varying the on time of the power switches. Resonant-mode designs achieve regulation by varying the switching frequency and fixing the power switches' on or off times.

The first major advantage of resonant mode comes from its sine-wave switching waveforms. In PWM, the switches turn off at high-current and high-voltage points. Thus, the PWM design's switch must dissipate a large amount of power during the switching transition. In contrast, resonant-mode techniques turn off their switches at either zero-current or zero-voltage points in the sinusoidal waveform; at either a zero-current or zero-voltage point, the switch's power equals zero. Therefore, the switching losses of resonant mode are much smaller than those of PWM designs. Resonant-mode designs also reduce switching stress on components because of reduced power-dissipation requirements. Further, resonant-mode techniques lead to reduced EMI and RFI, unlike PWM methods, because the fixed inductor and capacitor values of the

The term "resonant mode" doesn't refer to any particular power-supply topology, but rather to a whole class of topologies.

resonant tank generate only one, fixed-frequency sine wave that has greatly reduced harmonics.

Other benefits of resonant-mode techniques stem from their higher operating frequencies. The switching losses inherent to PWM designs allow practical switching frequencies of 400 or 500 kHz. The low-loss benefits of resonant-mode techniques start at switching frequencies of approximately 200 kHz and still apply at frequencies as high as 10 MHz, depending on the resonant-mode supply's topology. Zero-current and zero-voltage switching topologies have practical upper-frequency limits of 1 to 2 MHz and 5 to 10 MHz, respectively. Zero-voltage switching is effective at higher frequencies than zero-current switching because it produces less high-frequency switching losses. These higher switching frequencies result in smaller transformer and output-filter components and reduced output ripple. Also, the supply's transient response can be much faster than that of PWM because the feedback-loop bandwidth can be much wider. These features are particularly important if you're designing equipment for distributed-power systems. These systems generally require smaller, card-mountable power supplies that feature medium power—50 to 200W—in a low-profile, lightweight, low-EMI package.

The term "resonant mode" doesn't refer to any particular power-supply topology, but rather to a whole class of topologies (**Ref 1**). These topologies divide logically into related groups, as shown in **Fig 2**. This classification doesn't imply that rigid barriers exist between the various topologies; it simply points out how the various topologies originated. Because of the rapid de-

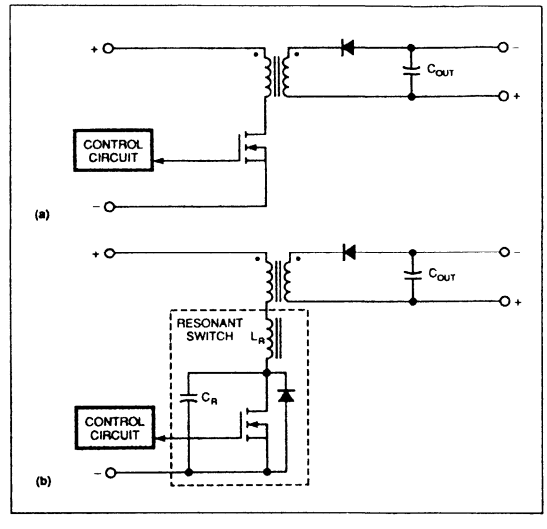

Fig 1—Resonant-mode circuits differ from PWM *because of the presence of two resonant components—an inductor and a capacitor. By adding C_R and L_R, you can convert the PWM half-bridge configuration shown in* ***a*** *to a resonant-mode design (****b****).*

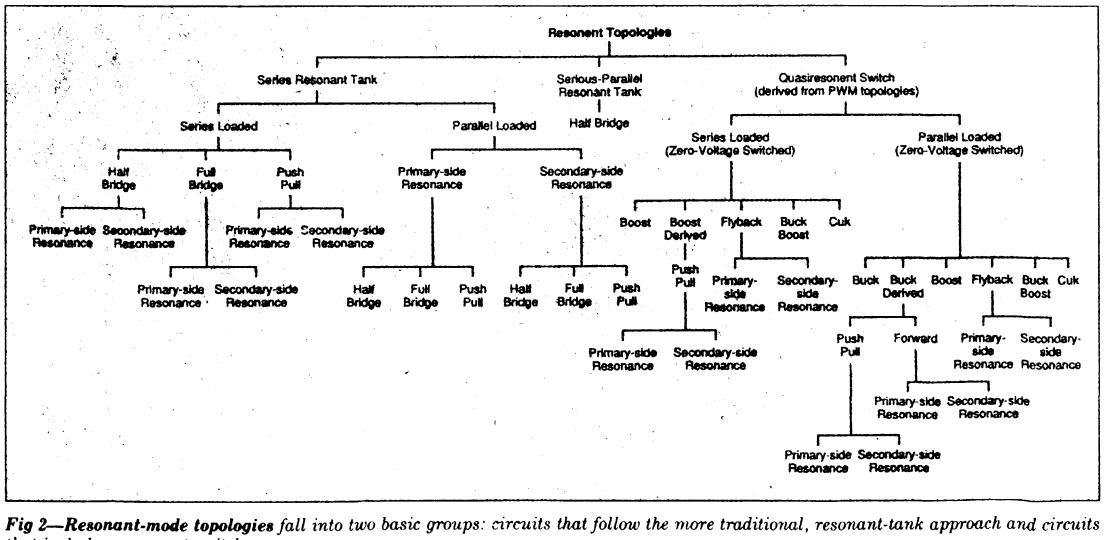

Fig 2—Resonant-mode topologies *fall into two basic groups: circuits that follow the more traditional, resonant-tank approach and circuits that include a resonant switch.*

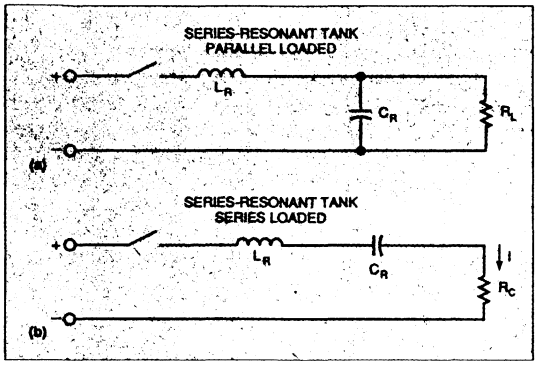

Fig 3—The connection between the tank and transformer *can be either parallel loaded* ***(a)*** *or series loaded* ***(b)***.

velopment of new topologies, the chart isn't exhaustive. The traditional topologies stem from the resonant-tank approaches and are shown under the "Series Resonant Tank" branch on the left side of **Fig 2**. More recently developed topologies rely on the resonant-switch approach and are shown on the right side of **Fig 2**, under "Quasiresonant Switch."

The designers who developed early resonant-tank approaches simply modified standard PWM topologies by adding a resonant tank. The resonant tank is usually series resonant; however, a hybrid, series-parallel tank connected in a half-bridge configuration does exist, as shown in the center branch of **Fig 2**. The next level of resonant-tank classification depends on the connection between the transformer and the resonant tank; the tank can be either series loaded or parallel loaded (**Fig 3**). The series-resonant, parallel-loaded converter traditionally is called a parallel-resonant converter.

The next level of resonant-tank classification concerns the type of PWM topology that each class of tank is based on—half bridge, full bridge or push pull. The circuits based on these various topologies differ according to the transformer type, the number and position of switches, the type of output rectification, and the normalized voltage and current stresses expected on all components.

Resonant mode and PWM are close relatives

The resonant-switch technique (**Ref 2**), shown on the right side of **Fig 2**, involves either a zero-voltage or zero-current resonant switch (**Fig 4**) inserted into a PWM-related topology in place of a normal switch. The resonant-switch topologies can replace the familiar PWM topologies, including the buck, boost, flyback, forward, and Cuk converters.

You'll notice further levels of classifications in **Fig 2** that divide all of these resonant-mode designs into either primary- or secondary-side resonance. Secondary-side resonance is accomplished by using the leakage inductance of the transformer as part of the resonant inductor and by moving the resonant capacitor to the secondary side of the transformer. However, primary-side resonance—the more commonly used technique—is simpler to perform.

So far, **Fig 2**'s classifications apply to the supply's transformer and resonant-tank connections. But the various methods of switch control shown in **Fig 5** also

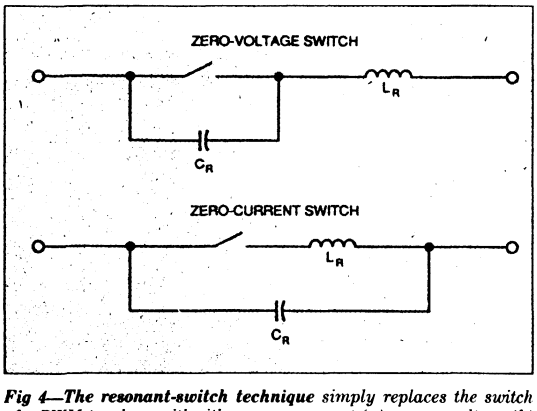

Fig 4—The resonant-switch technique *simply replaces the switch of a PWM topology with either a zero-current* ***(a)*** *or zero-voltage* ***(b)*** *resonant switch.*

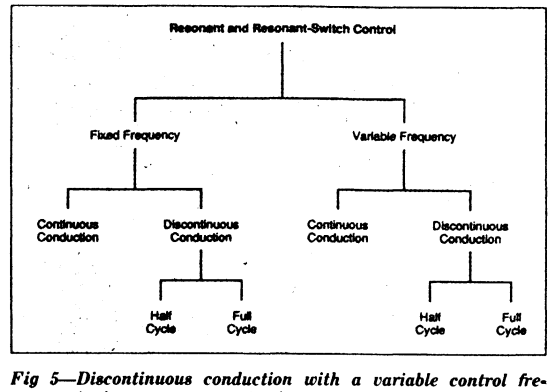

Fig 5—Discontinuous conduction with a variable control frequency *is the most common implementation of resonant-mode designs. Half-cycle conduction requires the use of a unidirectional switch; full cycle requires a bidirectional switch.*

Resonant-mode designs improve upon PWM techniques by allowing lossless switching at higher frequencies.

determine the supply's operation. If the switch control's frequency is equal to or greater than the resonant tank's natural frequency, the power supply operates with continuous conduction. In other words, the current will be flowing at all times through the resonant components. Continuous conduction is a valuable control method for high-power applications, but this method isn't desirable for most resonant-mode designs because it doesn't provide lossless switching.

Instead, most resonant-mode designs use discontinuous conduction. This condition occurs if the control signal's switching frequency is always below the resonant frequency. With discontinuous conduction, a dead time exists when no current flows in the resonant tank. The switch can either conduct current in one direction (half cycle) or bidirectionally (full cycle).

The circuit shown in **Fig 6** serves as a good example to illustrate the various cycles and required control signals of a typical resonant-mode design. This off-line power supply takes in 110V ac and produces 5V dc at 25A. This 5V supply's design is classified as a series-resonant LC tank with a parallel-loaded transformer and primary-side resonance in the half-bridge configuration. The design implements discontinuous-conduction control with full-cycle conduction. The controller turns off the switch at the zero-current point in the resonant inductor's current waveform.

Waveforms say it all

The waveforms in **Fig 7** illustrate the various intervals during one cycle of this supply's operation. In interval A, initially no current flows in the resonant inductor, L_R, and the voltage across the resonant capacitor, C_R, is zero. The output choke, L_2 (which is a large-value inductor), filter capacitor, C_{OUT}, and resistive load (not shown) collectively resemble a dc current

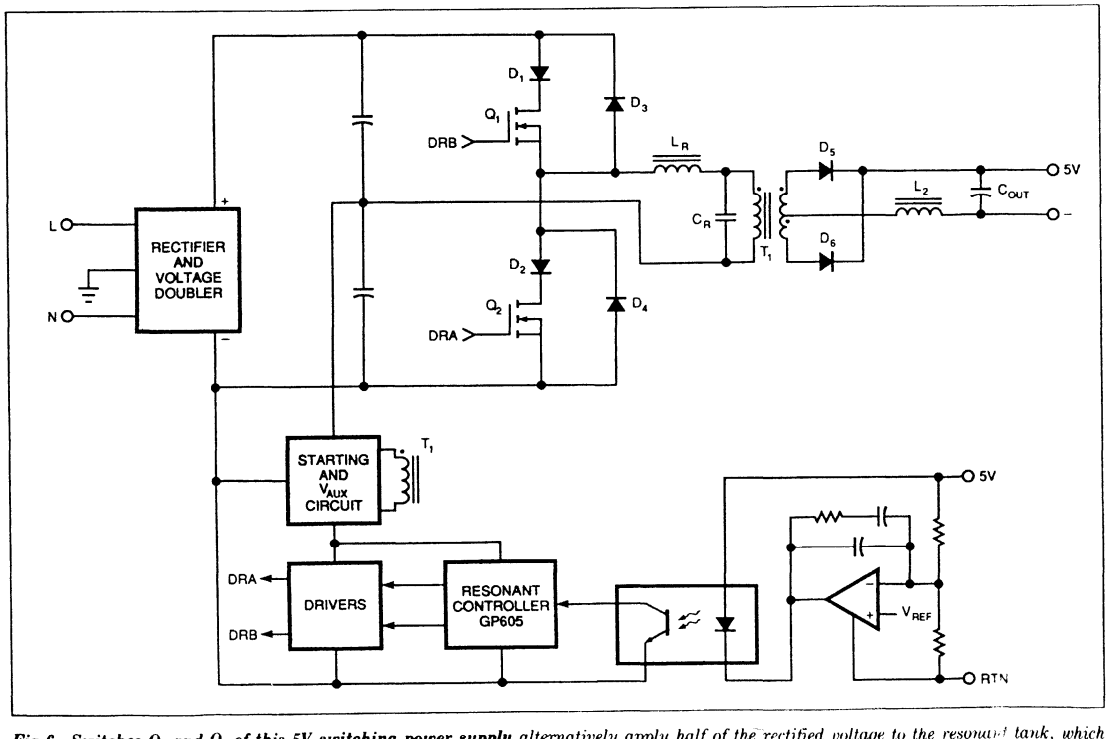

Fig 6—Switches Q_1 and Q_2 of this 5V switching power supply *alternatively apply half of the rectified voltage to the resonant tank, which comprises L_R and C_R. D_1 and D_2 are ultrafast recovery diodes that conduct the reverse current.*

Resonant mode's higher frequencies result in smaller transformer and output-filter requirements and in reduced output ripple.

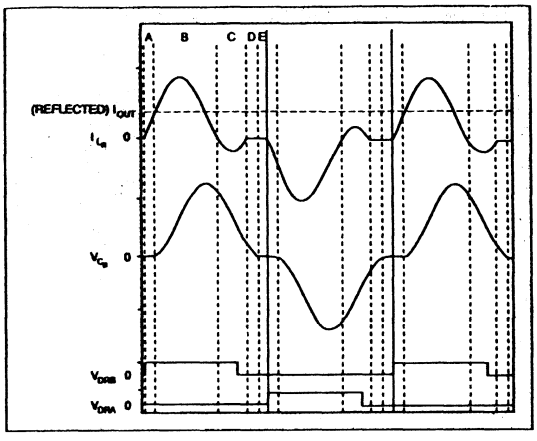

***Fig 7—These half-bridge, resonant-converter waveforms** illustrate the current, voltage, and control functions. Note the linear discharge of the resonant capacitor in mode D. The charge left on the capacitor varies with the line voltage. The slope of the discharge varies with the load current.*

load. This load causes both D_5 and D_6 to be on. When V_{DRB} goes high, Q_1 closes, and the current through L_R increases linearly until it matches the output-current requirements.

Interval B begins when C_R begins to charge. V_{CR} and I_{LR} are now sinusoidal in shape because of the resonant tank's action. The load acts as a constant current sink, so it doesn't affect the shape of I_{LR}'s or V_{CR}'s waveforms. The load's only effect is that it causes a dc shift in the current waveform. Note that I_{LR} isn't centered around zero.

Interval C begins when I_{LR} crosses through zero, and current starts to flow back from C_R into the inductor and back to the line. The transformer's primary is still taking from the dc current, which is needed to drive the output choke, from the resonant tank. The FETs, Q_1 and Q_2, although not actively turned off at the beginning of this interval, don't allow reverse current to flow because of their series-blocking Schottky diodes, D_1 and D_2. The antiparallel diodes, D_3 and D_4, carry the reverse current. During interval C, the controller must end the cycle by turning off Q_1's gate drive when the current waveform returns to zero at the end of its negative excursion; hence the name "zero-current switching."

At the end of interval C, I_{LR} is equal to zero, but the resonant capacitor still retains a positive voltage. In mode D, this voltage discharges to zero linearly because the output choke is acting as a constant-current load. In modes A, B, and C, the voltage applied to the output choke is equal to V_{CR} multiplied by the transformer's turns ratio, n. The turns ratio in this application is 1:12. The output-filter cap will try to minimize the ripple by providing current to the load, so in the modes A, D, and E, the choke current will be decreasing.

Interval E, known as the dead time, begins when the resonant capacitor is fully discharged. The freewheeling rectifying diodes, D_5 and D_6, prevent the output capacitor from being pulled below ground. Both D_5 and D_6 turn on to provide current to the choke.

Energy transfers to the output during the tank's resonant cycle (intervals A, B, and C); it also transfers just after the cycle is complete, while a positive voltage still exists on the resonant capacitor (interval D). After C_R discharges, there is a time when no energy conversion takes place (interval E). The conversion ratio—voltage in vs voltage out times the turns ratio—depends on the relative times of intervals A through D vs interval E.

Because the resonant-tank frequency is fixed, modulation of this dead time is an obvious way to regulate the output. By using an error amplifier to compare the output voltage to a reference, you can generate a signal to control the frequency of the GP605 controller. You can use the square pulses of fixed on-time outputs of

this controller to trigger the power FETs. The control pulses that turn on the FETs must occur one at a time, and the controller must insert a variable dead time between alternate pulses, as required by the resonant-mode scheme. This type of dual output is suitable for the gate drive of FETs in the half-bridge configuration.

As the load increases, the dc level of I_{LR} increases. The maximum amount of load current is available when the current waveform is just barely able to return to zero; that is, when I_{LR}'s negative peak during interval C is tangent to zero. Under this condition, no dead time (interval E) occurs. If the load (and therefore I_{LR}) increases to the point where the current can't return to zero, you lose all the zero-current switching benefits, and you'll have high losses. Therefore, you have to make a tradeoff between lossless switching and the amount of power supplied to the load. You must design the resonant tank so that I_{LR} has a swing large enough to fulfill your design's specifications. Part 2 addresses these design concerns and also examines the design of the control loop, resonant tank, and transformer in more detail.

Part 2 EDN November 23, 1989

Part II of this 2-part article on resonant-mode power-supply design techniques outlines the control-loop, output-filter, and transformer designs. By choosing components and safety margins so that your design satisfies all the requirements of zero-current or zero-voltage switching, and by paying attention to fault-control and start-up considerations, you can attain the benefits of the resonant-mode technique.

Although the block diagrams of quasiresonant-mode power supplies and the more familiar PWM power supplies are quite similar, both major and minor circuit differences exist that you must consider when designing the control loop and other support circuits. The control loop is a critical component of any power-supply design and greatly affects the supply's final specifications. These specifications include the load regulation, line regulation, load transient response, and stability of the output under all load and line conditions.

As with any design, you should quantify your resonant-mode supply's specification goals before you begin its design. To illustrate a detailed resonant-mode design, **Fig 1**, a very popular quasiresonant converter topology, shows a more detailed schematic of the off-line power supply used as an example in Part I. The target specifications of this half-bridge-configured supply are

- nominal input voltage: 110V ac
- output voltage: 5V at 25A
- minimum output current: 0.9A
- efficiency: approximately 80%
- maximum output ripple: 100 mV p-p
- line regulation: better than ±0.5% for inputs between 95 and 132V ac
- transient response: output settles to within ±5% in 500 μsec for a 50 to 100% step load.

In addition to these specifications, you also must choose the desired switching-frequency range. The fundamental requirement of quasiresonant converter designs—zero-current or zero-voltage switching—is that the switching frequency be lower than the resonant-tank frequency. This timing relationship ensures that a dead time will exist between cycles. The practical frequency limit of zero-current-switching resonant converters is approximately 1 MHz. At higher frequencies, you may have problems with the ferrite material currently available for resonant-mode designs. In the present example, the design goal for the resonant tank's frequency is 750 kHz.

To determine the maximum allowable switching frequency, you must establish timing relationships between the resonant and switching frequencies at both nominal and worst-case conditions. Under no-load conditions, the resonant tank's current and voltage waveforms look like **Fig 2a**; note that I_{LR}'s waveform is centered around zero. Under maximum-load conditions, the waveform looks like **Fig 2b**; note that here I_{LR} barely goes negative.

To guarantee zero-current switching under all line and load conditions, the current must reverse direction—go negative—for some period of time. Remember that the term "zero current" doesn't imply "zero crossover" switching. As long as the resonant inductor's current is negative, the switch carries "zero current" because the negative current flows through D_3 and D_4. You should design for a negative-current time that's equal to 25% of the full cycle under nominal conditions. You'll want the FET's drive pulse to turn off at the midpoint of this negative-current cycle, or at 87% of the resonant cycle's period. Thus, the desired on time for the switches in this design is 1160 nsec. **Fig 3** summarizes these timing relationships.

Unfortunately, tolerance variations in the resonant inductor and capacitor will always exist. The errors in inductor and capacitor values affect the tank's char-

To ensure lossless switching, the resonant frequency must be at least 20% higher than the switching frequency.

acteristic frequency in addition to the energy in the tank. If these variations shift the resonant frequency by too much, another resonant cycle may begin before the previous one has ended. If overlap occurs, the circuit operates in the continuous-resonance mode, and this mode's nonzero-current switching entails higher switching losses.

To ensure that the gate's drive pulse can't start another cycle unless the previous one is complete, add a 20% difference between the resonant frequency and the switching frequency. With this added margin, the controller's switching period will equal the resonant period plus 20%, or 1600 nsec. Thus, the controller's commutation frequency is approximately 600 kHz. Including a certain amount of dead time in your design also ensures that the resonant capacitor is completely discharged at the beginning of each cycle.

Once you know all your target specifications, you can choose specific component values for the circuit blocks of your quasiresonant-mode supply. **Fig 4**'s block diagram is representative of all off-line supplies. One main difference between quasiresonant-mode designs and more common PWM designs is the type of control. Most resonant-mode controllers implement a voltage-to-frequency conversion as opposed to the voltage-to-duty cycle conversion of PWM controllers.

Output filter is central to performance

One of the central elements of **Fig 4**'s block diagram is the output filter because it largely determines the power supply's frequency and ripple characteristics. In general, if the output filter's cutoff frequency is lower than the switching frequency, no high-frequency signals will corrupt the supply's output. As required in PWM designs, you must design the output filter so that the supply meets its output-ripple specification.

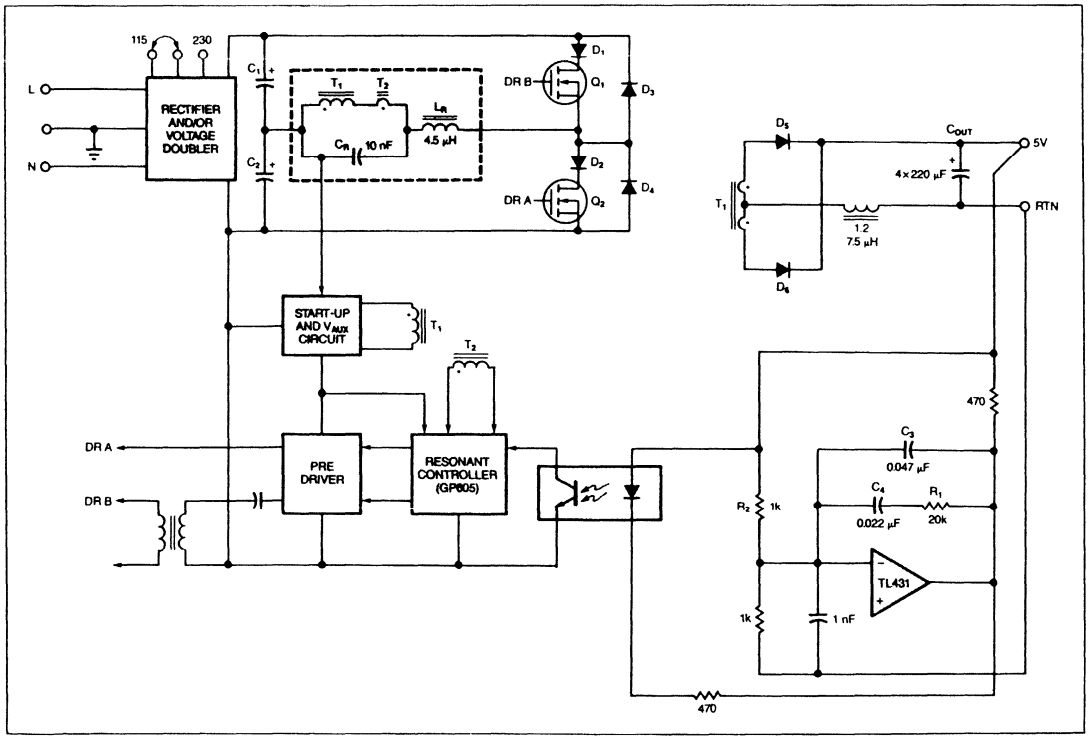

***Fig 1—Switches Q_1 and Q_2** in this 5V, resonant-mode power supply alternately apply half of the rectified voltage to the resonant tank, L_R and C_R. The ultrafast recovery diodes, D_3 and D_4, conduct the reverse current.*

One of the central elements of a resonant-mode design is the output filter, because it largely determines a supply's output-ripple characteristics.

In PWM supplies, the choke's ripple current is triangular, whereas in resonant converters the output current is sinusoidal because of the sinusoidal voltage on the secondary. The resonant converter's transformer secondary voltage is

$$V_{SEC}(1-\text{COS } 2\pi\, t/T_R)$$

where V_{SEC} is the peak dc voltage on the secondary, and T_R is the resonant period. The output inductor's voltage, therefore, is

$$V_{SEC}(1-\text{COS } 2\pi\, t/T_R)-(V_{OUT}+V_F)$$

during the resonant period. V_F equals the forward voltage drop of the output diodes, D_5 and D_6. When high currents flow through these diodes, V_F can be as high as 1V.

The worst-case ripple of resonant-mode designs occurs under the same conditions as in PWM designs but for slightly different reasons. The worst case for PWM designs is high-line and maximum-load conditions, because the duty cycle is low, and the output capacitor is discharging at its maximum rate. For resonant-mode designs, the worst-case ripple is also at high line and maximum load, because the switching frequency is low, and the rate of capacitor discharge is at a maximum.

The output-inductor current is approximately

$$I_L(t)=\int \frac{1}{L}\,[V_{SEC}-V_{SEC}\,\text{COS } 2\pi\, t/T_R - (V_{OUT}+V_F)]\,Dt$$

When you integrate equation 4 over the entire resonant period, the result is

$$IL_{PEAK}=\frac{T_R}{L}\,[V_{SEC}-(V_{OUT}+V_F)]$$

IL_{PEAK} is the peak ac current in the inductor. The dc current equals the output-load current. The turns

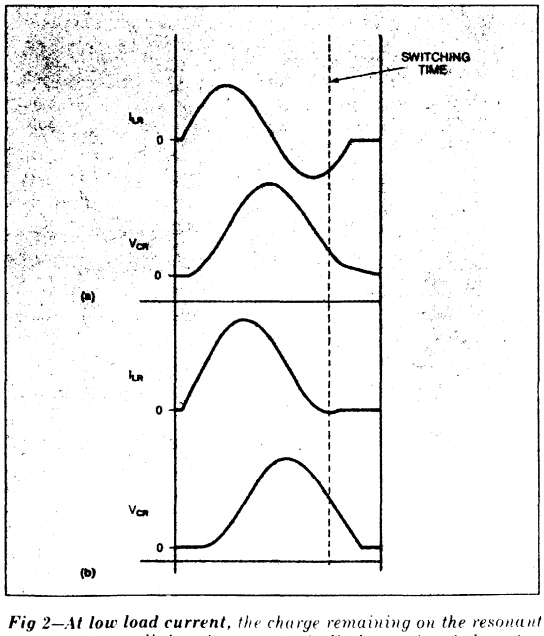

Fig 2—At low load current, *the charge remaining on the resonant capacitor is small, but the capacitor's discharge time is long* ***(a).*** *At high load current, the remaining charge is large (almost one-half the line voltage), but the high load discharges the capacitor rapidly to allow high-frequency operation* ***(b).***

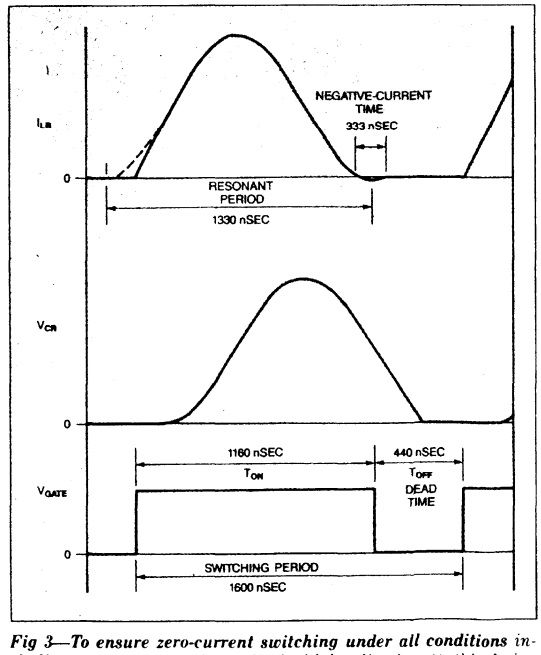

Fig 3—To ensure zero-current switching under all conditions *including worst case (maximum load with low line input), this design includes a 25% dead time (440 nsec) and at least 333 nsec of reverse-current time.*

The control loop of resonant designs uses voltage feedback rather than current feedback because the latter requires square-wave transformer signals.

ratio and the maximum input line voltage determine the value of the peak secondary voltage, V_{SEC}, as follows:

$$V_{SEC}=\frac{\sqrt{2}\ V_{LINE}}{\text{TURNS RATIO}}$$

For this design example, the high line is 132V rms, and the turns ratio is 12:1. Thus, the peak voltage on the transformer secondary is 16V. Choose the output inductor's value so that the inductor just barely conducts at the minimum load of the power supply. A rule of thumb is that IL_{PEAK} should equal at least $2\times I_{OUTMIN}$. For this design, therefore, $IL_{PEAK}=1.8A$. Using the above equation for IL_{PEAK}, you can solve for the minimum value of L. For this particular design, V = 16V, $V_{OUT}=5V$, $V_F=0.7V$, and $T_R=1330$ nsec. Thus, the minimum L is 7.5 μH.

You can use several approaches to find the minimum value of the output capacitor. One approach is to take the integral of the positive half cycle of the capacitor current to find the maximum charge—hence the maximum ripple—on the capacitor. This approach yields a vastly underestimated value for C_{OUT}, because it neglects the capacitor's equivalent series resistance. In most designs, the equivalent series resistance is the dominant factor that affects the capacitor's value. The effects of this resistance usually cause the required C to be approximately 10 times greater than the value you'd get using the integral approach. The maximum allowable equivalent series resistance is V_{RIPPLE}/IL_{PEAK}, which is 100 mV/1.8A or 55 mΩ for this design. To meet this requirement, the design requires four 220-μF, military-grade, low-equivalent-series-resistance capacitors connected in parallel, which reduces their combined equivalent series resistance.

Another important block in **Fig 4** is the error amplifier. Resonant-mode designs commonly use voltage feedback rather than current feedback. The conventional current-mode control used in PWM supplies isn't applicable to resonant mode (**Ref 2**), because it depends on the existence of a current ramp through the transformer. This current ramp occurs only if you apply a square-wave voltage to the transformer.

The feedback amplifier generates an error signal by resistively dividing the output and comparing the divider's output to a reference. This error amplifier, which uses the TL431CLP shunt regulator, also provides loop compensation. The transfer function of the amplification stage is

$$\frac{V_{OUT}(s)}{V_{IN}(s)}=\frac{s+1/R_1C_4}{sR_2C_3\left(s+\frac{C_3+C_4}{R_1C_3C_4}\right)}$$

C_3 is responsible for the first pole at 0 Hz, and it acts as an integrator to provide high dc gain for good dc regulation. The second pole is located at

$$f_2=\frac{C_3+C_4}{2\pi R_1C_3C_4}\ \text{Hz}$$

and a zero is present at

$$\frac{1}{2\pi R_1C_4}\ \text{Hz}$$

To avoid dc coupling, the output of the error amplifier drives an optocoupler that provides the necessary isolation between the transformer's primary and secon-

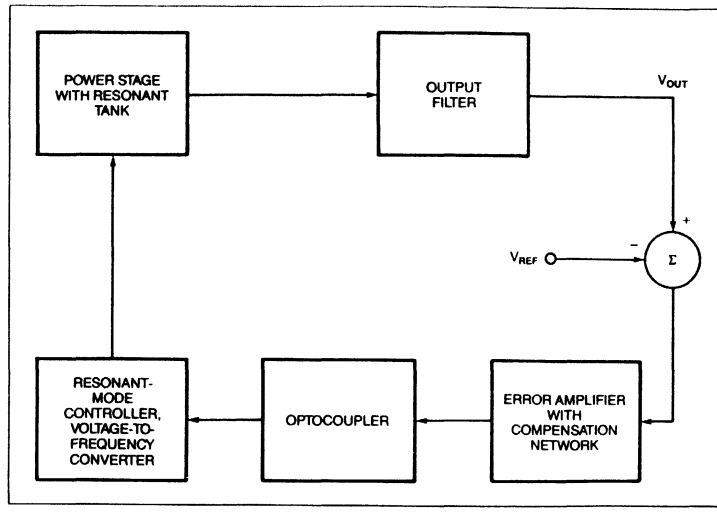

Fig 4—A resonant-mode power supply's control loop *contains the same functional blocks as do PWM supplies with one exception: a voltage-to-frequency converter replaces PWM's voltage-to-pulse-width converter.*

The components of the resonant tank simultaneously must provide enough energy to the output tank and limit the current through the FET switches.

dary sides. As with PWM designs, you can select the error-amplifier components and optocoupler gain to achieve the desired crossover point in the closed-loop response. The closed-loop crossover frequency for the overall control loop is 10 kHz; the phase margin varies between 47 and 94°, depending on line and load conditions.

As **Fig 4** shows, the optocoupler's output signal is the control voltage for the internal VCO of the resonant controller (GP605). The optocoupler and the controller each feature high gain, so they control the overall loop gain. The control IC's VCO generates a square wave at the operating frequency determined by the input signal. The controller divides the VCO signal into complementary phases (**Fig 5**). Then, the IC's internal monostable starts a fixed, on-time pulse at each edge of the main VCO square wave. The complementary square waves alternately gate this pulse to output A and output B. The controller accepts a voltage input and outputs a frequency. Thus, its gain is measured in Hz/V. The gain of the GP605 is linear between the minimum and maximum VCO frequencies. At the VCO's end points the frequency is clamped, and the gain drops to zero.

A restriction unique to resonant-mode designs because of the required zero-current switching is that the on time of the FET switch must be fixed. In zero-voltage switching, the off time is fixed. Most resonant-mode designs don't require this pulse width to be precise. For zero-current switching to occur, the controller can turn off the FET at any time during the negative-current cycle.

Because the control IC's output pulses are fixed, the controller can't react to variations in line or load once the pulse is triggered. Instead, the controller compensates for changes in output conditions by varying the start of the next pulse. This characteristic adds inherent phase delay to the feedback loop. The added phase shift equals 360° at the switching frequency. The switching frequency is always much higher than the loop bandwidth, so you can safely ignore the effect of this additional phase shift.

The GP605 controller generates high-current output pulses with a peak-current capability of about 800 mA using a totem-pole design. Usually this output current isn't enough to drive power MOSFETs directly unless the application requires less than 50W of power or a low input voltage. The current drive requirements of the FETs are very large because of the Miller multiplication of their gate-to-drain capacitances. As **Fig 1** shows, you can solve this problem by adding a predriver between the controller outputs and the power-FET inputs.

Resonant-tank design requires a balancing act

When you design the resonant tank—that is, when you choose the resonant inductor and capacitor values—you must fulfill two opposing requirements. First, enough energy must cycle in the tank to let the supply meet the load's energy demands. Second, your design must minimize the peak-current stress of the FET switches. The worst case for simultaneously fulfilling both of these requirements exists under low-line and full-load conditions.

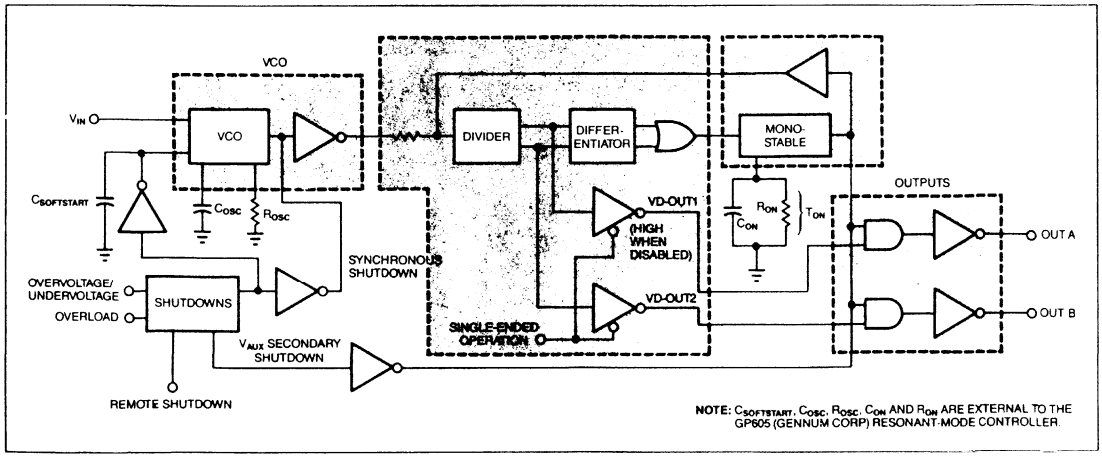

***Fig 5—The resonant-mode controller IC** (the GP605 from Gennum Corp) responds to voltage inputs and delivers a fixed-width pulse. The supply's output regulation occurs as the chip varies the frequency of this pulse based on the voltage feedback.*

For predictable operation at start-up and under fault conditions, make sure your supply has controllable open-loop characteristics.

The energy stored in the tank equals

$$\frac{C_R V_{PEAK}^2}{2}$$

where V_{PEAK} is the peak voltage across the tank capacitor.
At the maximum frequency, the power in the tank is

$$P_{TANK}=\frac{C_R V_{PEAK}^2 F_{MAX}}{2}.$$

Losses occur during energy transfer from the tank to the output; $P_{OUT}=P_{TANK}\times\eta$, where η is the efficiency. For this design, the absolute minimum input voltage—the input at which the tank is barely supplying power to the load—is 78V rms. Because of the voltage doubler on the input, the dc voltage applied across the entire tank is $2\times\sqrt{2}\times 78$, or 220V. By using $V_{PEAK}=220V$, $P_{OUT}=125W$, efficiency = 80%, and $F_{MAX}=600$ kHz, you can solve the above equation to find $C_R=10$ nF. You can then use the following equation to choose L_R so that the resonant frequency is 750 kHz:

$$L_R=\frac{1}{C_R 4\pi^2 F_R^2}.$$

For this example, L_R equals 4.5 μH.

The resonant transformer is different from a PWM transformer in that the applied voltage is a haversine wave and not a square wave. A haversine wave is a sine wave dc shifted so that its positive peak is at 2V, and its negative peak is at 0V (**Ref 4**). When calculating the turns ratio, account for this difference by using the average voltage of the haversine wave. The fact that the applied voltage is sinusoidal also affects the maximum operating flux density. The flux density in the transfomer equals

$$B_{MAX}=\frac{10^8}{NA_e}\int_0^{T_R} V_{PRI}\,Dt \text{ GAUSS}$$

where V_{PRI}, the primary voltage, equals $V(1-\cos 2\pi t/T_R)$; T_R is the resonant period; N is the number of turns on the primary; A_e is the transformer core area in square centimeters; and V is the maximum voltage applied across the resonant tank, or $\sqrt{2}\times V_{LINE}$. When you evaluate it over one complete cycle, this equation simplifies to

$$B_{MAX}=\frac{10^8 V T_R}{NA_e} \text{ GAUSS}.$$

Use this equation to calculate the core losses for your transformer design, and then check with the core manufacturer to ensure that the core losses are reasonable. Note that in this half-bridge example, the frequency applied to the core is approximately 300 kHz.

As long as the core isn't saturated, the high-frequency core losses result from hysteresis, residual, and eddy-current losses. Hysteresis losses are proportional to the maximum flux density times the frequency. Therefore, to increase the operating frequency from 10 kHz to 1 MHz, you'd have to divide the flux density by 100. Eddy currents are proportional to the square of the frequency, and thus at high frequencies, these currents cause a dramatic increase in losses. You can minimize losses by maximizing the ac core resistance, but this task usually requires special materials. The H7F material recently introduced by TDK is an efficient, high-frequency core material.

When designing the windings of a high-frequency transformer, you also must consider the skin effect. Normally, you'll want the secondary to have only a single turn. To minimize the skin effect, use copper foil for the secondary winding; either bifilar windings or copper foil is acceptable for the primary winding. Flat winding material is easier to work with if you etch the winding on a pc board, and then insert it onto the center leg of an E-core. This technique maximizes the utilization of copper, because the pc board's copper thickness is usually about twice the skin depth. This technique also minimizes fringing effects and leakage inductance because the windings are much wider than they are thick, and the thin profile allows very close coupling between the windings. Sandwiching the primary around the secondary also minimizes the leakage and improves the coupling.

Start-up and shutdown require open-loop stability

Although most of the circuit elements that correspond to **Fig 4**'s block diagram fulfill the control loop's closed-loop requirements, the open-loop stability of a power supply is also very important. Open-loop characteristics are especially critical when, for whatever reason, the feedback-voltage signal representing the error voltage lies outside the small-signal input range of the controller. The open-loop situation occurs at start-up and under fault conditions. Under these circumstances, a limit on the maximum frequency of the switch's drive waveforms is necessary. As long as the pulse width is still fixed, and you have control over the frequency, the operation of the supply will be predictable.

New High Performance ZVS Resonant Mode Controller

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ABSTRACT

High frequency resonant mode designs are becoming more and more popular to overcome the switching losses present in PWM designs. Up to now, the category of Zero Current Switched (ZCS) topologies has been the most popular , mainly because of well documented operation and the availability of several dedicated resonant controllers. But lately there is high interest in the Zero Voltage Switched (ZVS) topologies as they have distinct advantages for operation at even higher frequencies than that possible with ZCS. One factor limiting the changeover to ZVS is the lack of a dedicated resonant mode controller that meets the requirements of this topology.

In this paper the ZVS concept will be briefly described outlining the differences between ZVS and ZCS, then the GP6140/ GP6141 resonant controllers from GENNUM will be introduced as integrated controllers that meet these unique requirements.

INTRODUCTION

Resonant mode, where the input current and voltage are shaped by an inductor and capacitor to approximate sine waves allows the switching of the power switch at either the zero crossing of the voltage waveform or the current waveform. If the topology uses switching at the zero current crossing it is a ZCS topology. If switching is at the zero voltage crossing it is ZVS topology. ZVS has benefits of eliminating the problem of switch parasitic capacitance, reducing the frequency deviation with wide load range and, due to high frequency operation, allowing the reduction of size/price of the converters.

FEATURES/REQUIREMENTS FOR ZVS CONTROLLER

In Zero Voltage Switching topologies the resonant capacitor is in parallel with the power switch (usually a MOSFET transistor). Such a configuration allows the parasitic capacitances to make-up part of the resonant capacitor (Fig 1). Due to zero voltage switching of the MOSFET transistor, the parasitic capacitance does not discharge violently through the MOSFET R_{DS} resistance, but takes part in the resonant action. The power switch therefore should remain OFF during the positive voltage swing on the power transistor, turn ON during the negative part of the sinusoid and remain ON for the remaining variable part of the cycle. The controller must set the proper "fixed" pulse width based on the designed resonant period. As explained, in ZVS the fixed pulse width represents the OFF time of the power switch. Two techniques are possible,

1) A zero crossing detector to terminate the pulse when the positive part of the resonant period has ended.

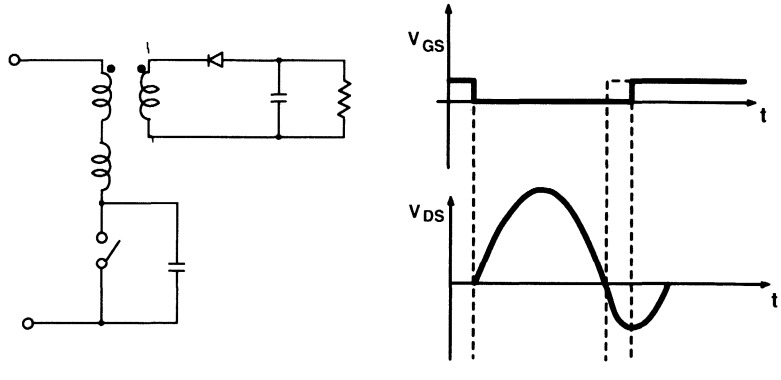

Fig. 1 ZVS Converter

Disadvantages
- complicated internal circuit reflecting controllers high price.
- sensitive to noise conditions in the zero voltage sensing circuits.
- require external sensing circuits
- in some conditions the sensing circuit may never detect the zero.

2) A monostable to generate fixed T_{OFF} pulse width preset by the external components.

Disadvantage
- the tolerances of the resonant tank and time setting components have to be very carefully calculated.

Industry price sensitivity makes the second solution more attractive.

Requirement: In the active condition, the controller should produce a variable frequency fixed T_{OFF} time waveform. During fixed T_{OFF} time the power switch should be in the OFF condition. The variable frequency should be controlled by an external pin (the power switch is ON during this period of time).

In the startup or shutdown conditions the controller should keep the power switch in the OFF state.

Requirement: In the stand-by condition, the controller should turn off the power switch.

In the V_{CC} undervoltage condition the controller should save energy by lowering down the power consumption.

Requirement: In the stand-by condition, the controller should have low quiescent current.

Following the standby condition the controller should ramp down the frequency from maximum to the frequency required by the feedback loop. The ratio between maximum to minimum frequency at preset condition does not have to be higher than 10.

Requirement: The rate of the frequency change during the start-up condition should be preset by the external components.

Requirement: On the start-up the frequency should decrease from maximum to that set by an external signal at a controlled rate.

For wide load range, the ON time of the switch, has to be very small compared to the fixed resonant OFF time. This is because of the ability to have very small ON time at the maximum frequency. Lack of the ON time is not allowed because the converter would revert to its OFF state with the resonant capacitor charged. The controller must guarantee a minimum ON time to ensure that the voltage will continue to resonate to zero. Maximum frequency accuracy is not critical since this determines minimum load. The minimum frequency controlling maximum load must be highly accurate for safe operation under open loop conditions.

Requirement: The minimum and maximum frequency should be set accurately by the external components.

Feedback is normally voltage mode feedback. Therefore the controller needs a control input normally made compatible with opto-coupler output for the isolation of the feedback error signal. The response to this feedback signal does not need a fast slew rate but the small signal response must be fast so that there are no delays added into the feedback loop causing instability. The delay due to the controller is usually negligible when compared to the overall phase delay caused by the output filters, error amplifier, and opto-coupler.

It is good to have a certain amount of bandwidth limitation in the control input circuitry so that there is less likelihood of responding to noise and amplifying its effect.

A simple 4 MHz Error Amplifier could be incorporated into the controller for an additional few cents. However the majority of applications require very specific kinds of feedback loop designs and usually the internal Error Amplifier is not used. Therefore it is omitted in this design.

Requirement: The feedback input with a small amount of bandwidth limitation is required.

On the first change of the output state after standby or shutdown condition, a large voltage and current must be applied to the switch to minimize power dissipation. To accommodate this function the drivers should be optimised to handle the capacitive load. However at 3 MHz frequency, with package dissipation of 700 mW, the maximum value of the capacitor that could be driven is 400 pF (due to capacitive charge and discharge in the driver transistors). Therefore there is the trade-off between the price, power dissipation, and maximum current available from the drivers.

Requirement: The current capability of the controller should be optimised for price and ability to drive the power MOSFET's.

The large voltage on startup condition is obtained by providing V_{CC} undervoltage shutdown.

Requirement: Vcc undervoltage shutdown.

The handling of faults is extremely important in the actual

application of the controller and can determine such things as the reliability, safety and controllability of the power supply within the system. This controller should have all proven features of the GP605 controller namely:

- overvoltage/undervoltage shutdown
- overload shutdown
- remote shutdown
- V_{CC} undervoltage shutdown

THE ZERO VOLTAGE SWITCHING CONTROLLER

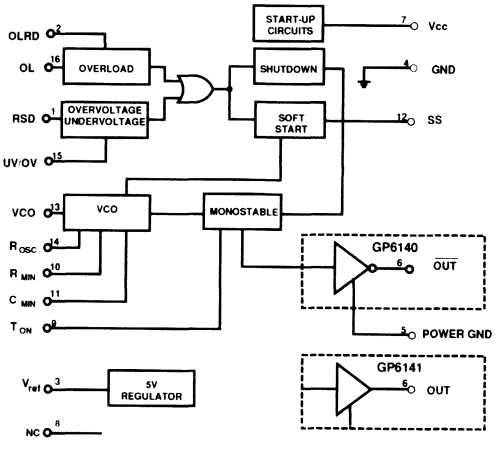

Fig. 2 GP6140 Block Diagram

The GP6140 contains a VCO, Monostable, and Power Output Stage (Fig 2) for the core function of taking the input voltage signal and producing a frequency dependent train of fixed off time pulses. Peripheral features added to make the controller versatile with a minimum of external parts include the Undervoltage/Overvoltage shutdown, an overload shutdown with delayed restart, a remote shutdown, and a soft-start delay for recovery from all shutdowns.

CORE FUNCTION OF GP6140

The GP6140 and GP6141 are designed for the common use of a controller on the primary side of an isolated power supply although they are acceptable for secondary side control as well. The input to the VCO is the feedback error voltage from the voltage sensing of the power supply output. The VCO input is made compatible with the output of an opto-coupler to simplify the feedback circuitry and to minimize noise interference. The VCO input controls the frequency of a square wave which is the input to the monostable. The monostable generates a fixed pulse width for the off time of the power switch. The monostable pulse controls the high current output stage that produces a high voltage pulse capable of driving power FETs directly. On startup the soft-start capacitor is used to ramp the frequency from maximum frequency down to minimum frequency as required by a ZVS controller so that energy transfer starts from minimum and increases to the amount required as set by the feedback voltage. The waveforms for the control path of the controller is shown in Fig 3 with the effect of a change in VCO control voltage. Low current startup allows well controlled startup conditions with no glitches, as well as providing low quiescent current when the IC is off. Shutdown, using any of the various ones available will disable the output in the off state so that the power switch is turned off. Other blocks important to the internal operation of the controller are the regulator and low current start up timing circuitry.

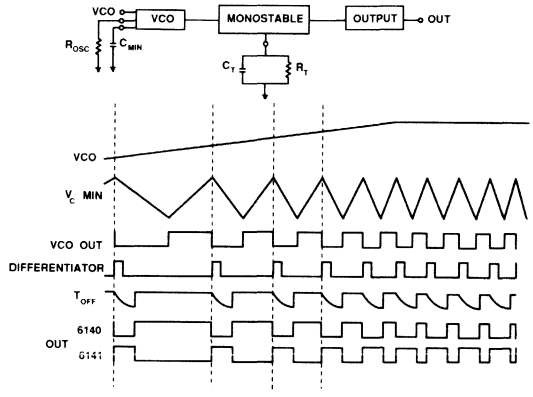

Fig. 3 Control Circuit

To have a high performance part the main control path which is composed of the VCO, Monostable, and output driver have to be designed with emphasis on precise timing and low delays. For ZVS topologies the controller must be able to drive the power FETs at frequencies above 2 MHz with very small ON times. Obtaining this in the IC design was with high frequency STL logic with ECL logic being used in extremely critical areas. Meeting the ZVS demand for precise control over the frequency was obtained with the ability for the user to externally set the precise values for the maximum frequency and the minimum frequency independent of each other. This was implemented with a unique design of a variable controlled oscillator and a high frequency monostable.

OPERATION OF CRITICAL BLOCKS

The detailed function of the VCO, monostable, output stage, and shutdown features will be given with the emphasis on the external to IC interface and how the unique features of this controller family can improve the design of ZVS power supplies.

Voltage Controlled Oscillator

The first stage of the VCO is the Voltage-to-Current Converter (Fig 4) that senses the control voltage input on the VCO pin and converts that value into a current. The relationship between the VCO voltage and control current is very linear for precise

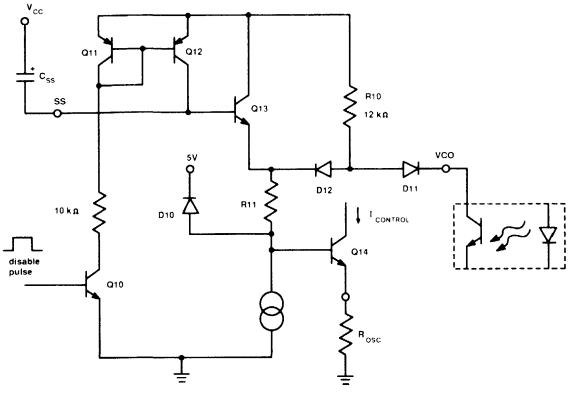

Fig. 4 Voltage to Current Converter (with Soft-start)

control of the feedback loop gain which is important to guarantee loop stability. When the VCO input goes beyond the input control range the power supply is basically operating open loop. In this situation it is critical to accurately control the power FETs to prevent improper operation. The Voltage-to-Current converter has accurate clamps designed-in for the maximum and minimum currents, which clamps the maximum and minimum frequency. The maximum current is

$$I_{MAX} = \frac{V_{REG}}{R_{OSC}}$$

since D10 clamps to the regulated line and cancels out the effect of the V_{BE} of Q14. R10 provides pull-up current for the opto-coupler. The requirement of soft-start is to override the VCO control voltage on startup to sweep the frequency from maximum down to the level set by the feedback loop. The SS pin normally has a resistor connected to ground and capacitor connected to V_{CC}. Under normal operation Q10 will be off keeping the C_{SS} capacitor discharged so that the VCO controls the current. If a shutdown is triggered the disable pulse to Q10 discharges the C_{SS} to the supply voltage. On removal of the shutdown condition the IC output will be enabled with Q13 on and clamping via D10 to the 5V rail. As C_{SS} discharges the frequency will decay from maximum until Q13 turns off and D12 turns on returning control back to the VCO input signal.

The Oscillator (Fig 5) operates on the principle of linearly charging and discharging an external capacitor (C_{MIN}) with precise current sources. This makes the waveform on C_{MIN} a triangle wave that swings between an upper and lower threshold. When C_{MIN} is charging the opamp negative terminal is referenced to V_{REG} by the resistor divider R_A and R_C,

$$\frac{R_C}{R_A + R_C} \quad V_{REG} = \quad 0.6\, V_{REG}$$

since V_O is low keeping both Q5 and Q6 off. This keeps Q3 of the differential amplifier off allowing the Iref current to charge C_{MIN}. Upon reaching the upper threshold Vo goes high which turns on Q6 and Q5. Q5 makes the new threshold derived from the resistor divider of Ra in series with the parallel combination of R_B and R_C.

$$\frac{R_B \text{ II } R_C}{R_A + (R_B \text{ II } R_C)} \quad V_{REG} = 0.3\, V_{REG}$$

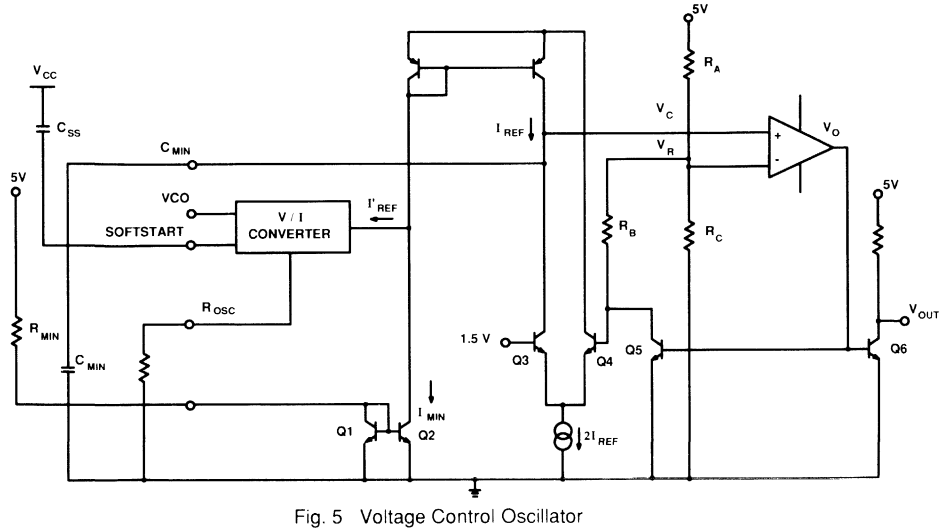

Fig. 5 Voltage Control Oscillator

Q3 is now ON with a collector current of exactly twice I_{REF} causing C_{MIN} to be discharged by a current of I_{REF}. Special techniques have been used in the creation of I_{REF} to keep the charging and discharging currents to be exactly equal even over processing and temperature variations. The equation for the oscillator frequency is

$$f = \frac{I_{REF}}{2 \times C_{MIN} \times (V_{HI} - V_{LOW})}$$

where $V_{HI} = 0.66\ V_{REF}$

$V_{LOW} = 0.33\ V_{REF}$

and $I_{REF} = \frac{V_{CO} - 1.2}{R_{OSC}}$

Very accurate f_{MAX} is obtained with this VCO since the maximum frequency is referenced to V_{REG} and so are the thresholds on C_{MIN} resulting in an equation for Fmax of

$$f_{MAX} = \frac{\frac{V_{REF}}{R_{OSC}}}{0.66\ V_{REF} \times C_{MIN}} \quad \text{or} \quad f_{MAX} = \frac{1.5}{R_{OSC} \times C_{MIN}}$$

This makes f_{MAX} dependent only on externally selected values eliminating any sensitivity to IC parameters.

The minimum frequency is also made independent of IC parameters since the minimum current is defined by the external resistor R_{MIN} connected to V_{REG}. By utilizing this technique we have eliminated the need to trim parameters in the manufacture of these controllers.

The independent control of the minimum frequency has been optimized for ZVS designs where a relatively narrow range of frequency is desired. The extremely wide range of ZCS designs, sometimes as wide as 1000:1 isreplaced by a typical range that rarely goes beyond 10:1. Designing a controller for both the ZVS and ZCS requirements clearly compromises the ultimate controller design because of the conflicting requirements.

The output of the VCO section is a square wave at the same frequency as the triangle wave on C_{MIN}. This square wave becomes the input to the monostable.

Monostable

From the falling edge of the input square wave a very narrow trigger pulse is generated by the Differentiator (Fig 6). This pulse sets the monostable latch which starts the output pulse as well as turning off Q27. The duration of the output pulse is set by the discharge of C_T by R_T. Initially C_T was charged to a V_{BE} below V_{REG} by Q27. With Q27 off the voltage on T_{OFF} will exponentially decay until the 1.5 V threshold is reached. Then Q24 would reset the latch which in turn terminates the output pulse and recycles the C_T capacitor in preparation for the next pulse. This gives the characteristic exponential decaying curve found on the T_{OFF} pin of the controller. The lower threshold is set to 1.5 to make sure that there is still a significant slope to the waveform so that precision is excellent and there is less susceptibility to noise. By keeping the lower trigger threshold,

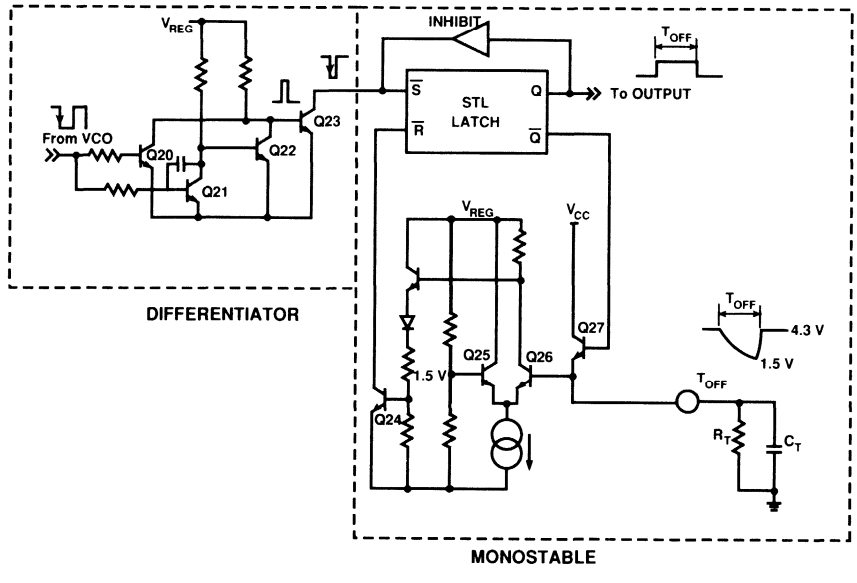

Fig. 6 Differentiator and Monostable Circuits

as well as the peak level on the C_T capacitor, proportional to the V_{REG} line, the resulting pulse width is largely independent of the V_{REG} accuracy or any other parameters of the IC. The only IC property that does affect the pulse width is the matching of resistor ratios which has been made small with judicious design techniques and the delays through the latch which have been minimized by using high speed Schottky transistor logic.

Zero Voltage switching designs require a fixed off-time pulse with good control. This monostable produces this well controlled pulse as well as a feature that prevents the VCO from overriding the monostable. If the maximum frequency is set improperly and a trigger comes before the monostable pulse is
complete the inhibit buffer prevents that pulse from having any effect. This ensures the power FET will be turned on at the zero crossing point regardless of the frequency to prevent unstable and unpredictable operation of the power supply. If the VCO continues to increase in frequency beyond the point where the inhibit has activated, the trigger pulse will be lost and the monostable will not trigger until the VCO sends another pulse. This creates an effective divide by two of the frequency which preserves zero crossing switching as well as being useful for power supply current foldback in some situations.

Output

The ZVS controllers described here are the single-ended versions so that the pulse from the monostable does not have to be delayed through several gates of steering logic but can be directly connected to the output stage for minimum propagation delay. The train of pulses from the Monostable triggers the output with the fixed time that the output stage is off (Fig 7).

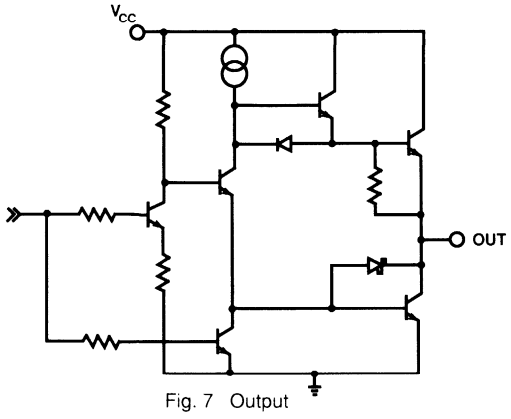

Fig. 7 Output

The variable frequency causes the output to be on for varying amounts of time which is the required operational mode of ZVS controllers. The shutdown or OFF mode of a ZVS controller is the fixed time state of the output which is opposite to a standard ZCS controller, where the OFF mode is the variable time state of the controller. It is this difference that makes it difficult to adapt ZCS controllers to ZVS power supply designs.
The output is a high current totem pole output stage that can directly drive power MOSFETs. The peak current capability of 1.6 A means switching a 100 pF load in about 10 ns. The output stage is made highly efficient by the use of a large area Schottky on the low side transistor which eliminates all crowbar or flow-through current.

For high frequency power supplies above 1 MHz, the limitation on whether the controller can drive a power FET directly is no longer determined by the peak current capability, but rather by the thermal coefficient of the controller package. Power FET gate-drives are notoriously capacitive with nonlinear capacitance at maximum when the drain-gate voltage is negative. By using low thermal coefficient packaging, the ZVS controllers have maximized their usability at these high frequencies . For versatility these controllers come in two versions, where the output is either active high or active low. The GP6140 has active low output providing direct drive, and the GP6141 has active high output suitable for predriver operation in larger power supplies.

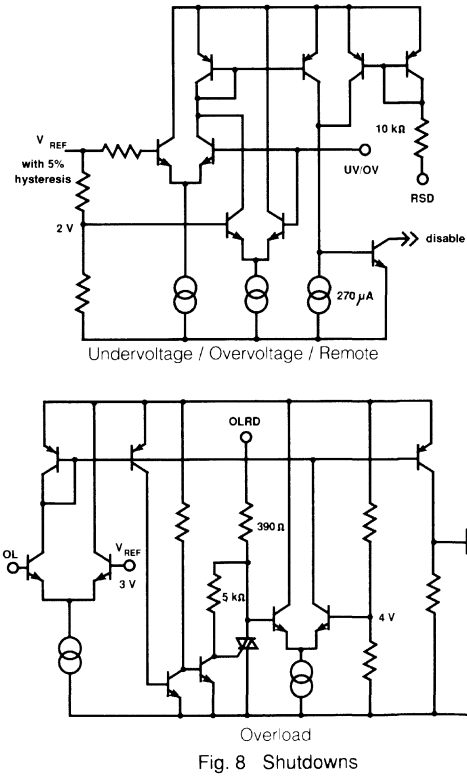

Fig. 8 Shutdowns

Shutdowns

Along with high performance power supplies that require high performance control, there is also a need for high performance peripheral features. The shutdowns on the GP6140/GP6141 are numerous and versatile, and require a minimum of external components. (Fig 8).

Undervoltage / Overvoltage / Remote

A window comparator is provided on-chip that uses the internal regulator to generate a 3 V reference that has 3% hysteresis at the trigger level. When the signal on the UV/OV pin goes outside the window of 2 V to 3 V the PNP current-mirror turns on, causing the disable transistor to turn on. This disable signal is propagated to various locations in the chip. The output stage is shut down directly for fast speed, and the soft-start capacitor C_{SS} is charged in preparation for the re-enable of the controller.

The remote shutdown input can be controlled either by a voltage input, or a current. If the current being pulled out of the PNP mirror exceeds 270 μA, the disable signal is generated. This corresponds to a voltage drop across the 10 kΩ resistor of 2.7 V. Since remote shutdown does not have hysteresis it is normally used with an external open collector transistor.

Overload

The overload shutdown also has hysteresis of 3% from a nominal threshold of 3 V. The signal generated by exceeding the threshold is transmitted to another disable transistor that immediately shuts down the output stage as well as discharging the soft-start capacitor. The second collector of the PNP mirror is used to trigger an SCR type latch which charges the capacitor on the overload restart delay pin to zero, at which time the latch resets itself. The capacitor will stay charged at zero volts as long as the OL threshold is exceeded. Upon dropping below the overload threshold the latch will release and allow the capacitor to discharge up to V_{CC} via the external resistor. The comparator will turn off the disable signal as soon as the 4 V threshold is exceeded,keeping the controller disabled as long as the OLRD capacitor is below 4 V. When the threshold is above 4V, the output is enabled in soft-start mode.

The waveforms shown in Fig. 9 represent the output pulses that are generated when the Overload input is triggered and the OLRD pin has a capacitor and resistor connected to V_{CC}. The waveforms for Overvoltage/Undervoltage would be similar but that there would be no Overload Restart Delay (OLRD).

Low Current Startup

In keeping with most commercially available controllers the GP6140 family has V_{CC} undervoltage lockout with low current startup. The wide range of hysteresis encourages the use of trickle charge startup for off-line supplies. When below the threshold, the controller has the regulator disabled as well as the output. Where there is high dv/dt on the V_{CC} line as in DC-DC converters or battery applications, direct disable of the output is required because the output must be guaranteed off until proper controller activation. High dv/dt would cause random and possible destructive output stage activation.

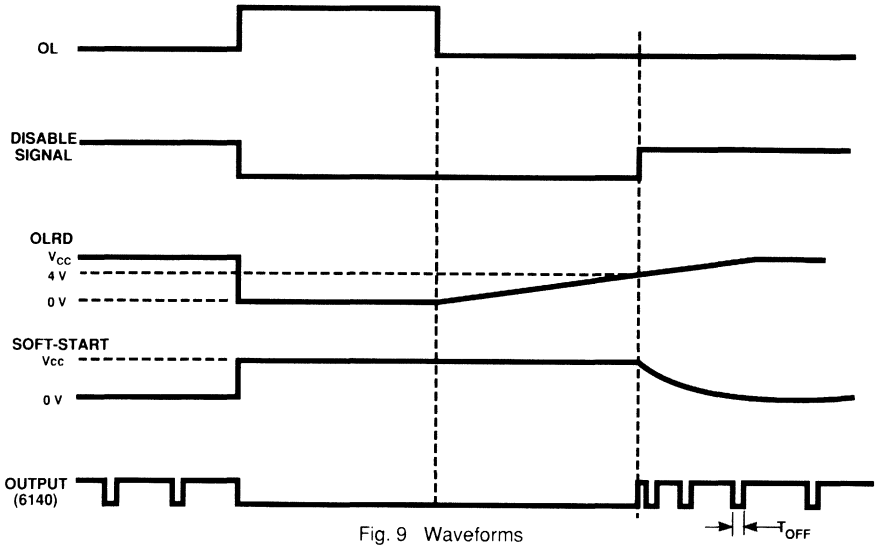

Fig. 9 Waveforms

CONCLUSIONS

In the comparison of ZVS to ZCS topologies it becomes clear that the respective controller requirements are quite different. The ZVS topology has been analysed to obtain the optimum controller features, resulting in the development of the GP6140 family of controllers. These controllers are shown to have high performance and versatility, with ease-of-use a definite advantage.

ANALOG ASICs & IC ARRAY PRODUCTS

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- Reduce your product size
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- **reduced PCB size**

For complete information about Gennum linear array products, please refer to our Semicustom Design Manual. Kits and manuals are available from Gennum or your local representative.

CIRCUIT DESCRIPTION

The Gennum semicustom integrated circuits are arrays of bipolar transistors, p diffused resistors, pinch resistors, junction capacitors and Schottky diodes. The individual components on the chip are uncommitted.

The user can design his own proprietary circuit using the transistors, resistors, and capacitors available on the chip. Once the circuit is designed and tested with discrete components (provided with the design manual), the interconnection layout is generated and used to manufacture the proprietary circuit.

SEMICUSTOM BIPOLAR ARRAY COMPONENT LIST (20 V MAX. OPERATING VOLTAGE)

		LA250			LA200		
ACTIVE COMPONENTS		L A251	LA252	LA253	LA201	LA202	LA204
Small NPN	- standard	122	92	52	83	46	17
	- Schottky clamped	18	12	8	-	-	8
	- low noise	8	8	8	-	-	-
	Total	148	112	68	83	46	25
Large NPN	-Ic ≤ 100mA	-	-	2	2	2	2
	- Ic ≤ 300mA	4	4	-	-	-	-
	Total	4	4	2	2	2	2
Lateral PNP	-split collectors (2)	36	24	16	26	14	9
	-multiple collectors (6)	13	10	4	-	-	-
	Total	49	34	20	26	14	9
Zener Diode		4	4	4	1	1	1
Large Diode		2	2	2	-	-	-
PASSIVE COMPONENTS							
Junction Capacitor	- 75 pF capacitors	4	4	4	3	3	-
	- 56 pF capacitors	-	-	-	-	-	3
	Total	4	4	4	3	3	3
Various P-Diffused Resistors (total resistance)		1000 K	670 K	340 K	450 K	240 K	170 K
40 K Pinch Resistors		28	28	20	10	8	6
BONDING PADS		40	32	24	24	18	14
CHIP SIZE (mils)		150 x 144	151 x 111	92 x 111	127 x 94	78 x 94	56 x 91

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GENNUM CORPORATION P.O. Box 489, Stn A, Burlington, Ontario, Canada L7R 3Y3 tel. (416) 632-2996 fax: (416) 632-2055 telex: 061-8525
Tokyo Office: 301 Aoba Building, 3-6-2 Takanawa, Minato-ku, Tokyo 108, Japan tel. (03) 441-2096 fax: (03) 448-8991

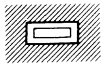
ULA COMPONENT DESCRIPTION

Legend for component drawings


Metallization


Contact


Emitter

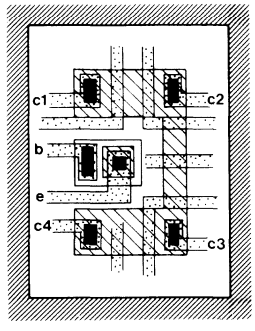

Base and Isolation

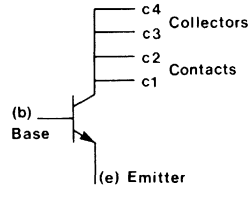

Base and Isolation in Zener Structure


DeepCollector Diffusion

Small Emitter NPN

The most common circuit element in the array and the one around which the process is optimized is the small npn cell. Since it is the most common cell, it makes sense to include the basic structure to implement cross-unders right in the layout. This is accomplished by making use of the low resistance emitter diffusion which forms the wrap-around collector structure, so that connections made to an npn collector on the circuit schematic may be made to any of the 4 collector contacts. It is not necessary for a particular npn to be used in the circuit before it can be used to implement a cross-under, in which case the transistor collector behaves like a low value resistor. In this mode, the base and emitter contacts should be shorted together.



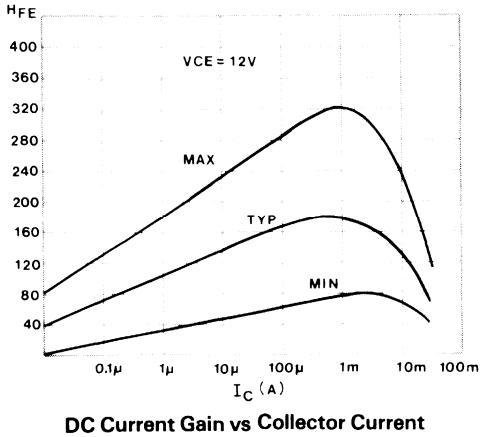


Small NPN Characteristics

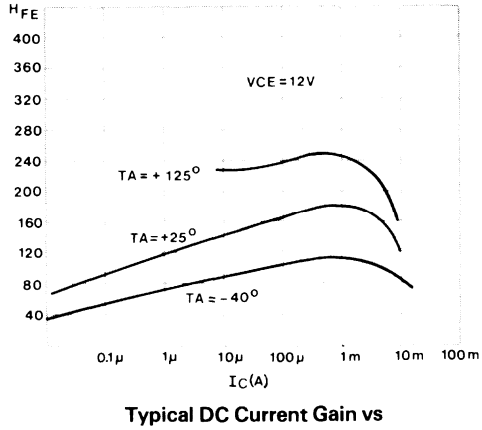
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
H_{FE}	I_C = 1 mA, V_{CE} = 12 V	80		320	
V_{BE}	I_C = 10 μA, V_{CE} = 12 V		600	640	mV
$V_{CE(SAT)}$	I_C = 10 mA, I_B = 1 mA		270	400	mV
	I_C = 1 mA, I_B = .1 mA		100	200	mV
BV_{CEO}	I_C = 20 μA, I_B = 0	20	27		V
BV_{EBO}	I_E = 20 μA, I_C = 0	6.5	7.5		V
I_{CEO}	V_{CE} = 12 V		10		pA
I_{CBO}	V_{CB} = 12 V		5		pA
V_A	I_B = 10 μA, V_{CE} = 5 V and 15 V	50	100		V
C_{OB}	f = 1 kHz, V_{CB} = 0		3.5		pF
f_T	I_C = 3 mA, V_{CE} = 12 V		250		MHz

ΔV_{BE} for adjacent devices 2mV typ (5mV max)

NPN Graphs

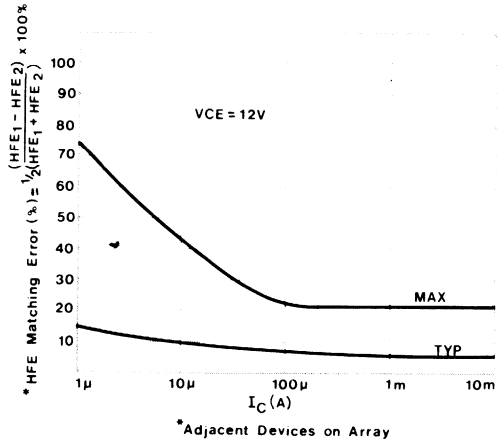


DC Current Gain vs Collector Current



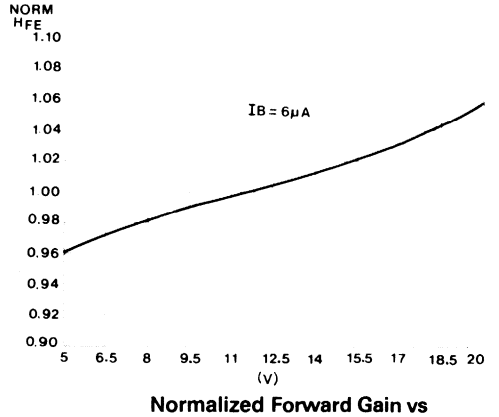
Typical DC Current Gain vs Collector Current over Temperature

NPN Graphs (continued)

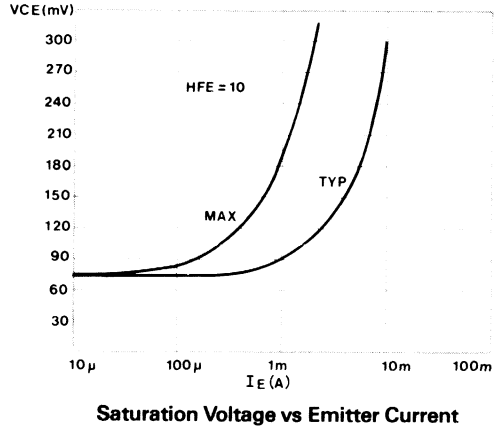


*Adjacent Devices on Array

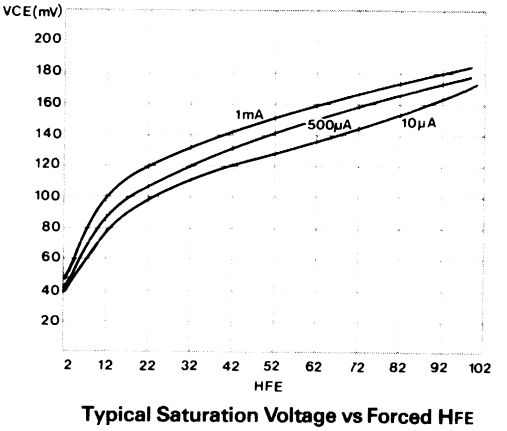
H_{FE} Matching Error (%)



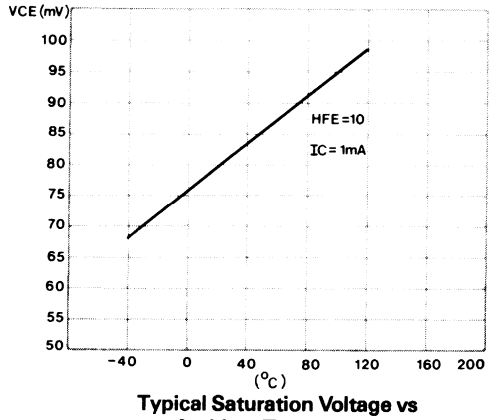
Normalized Forward Gain vs Collector Voltage



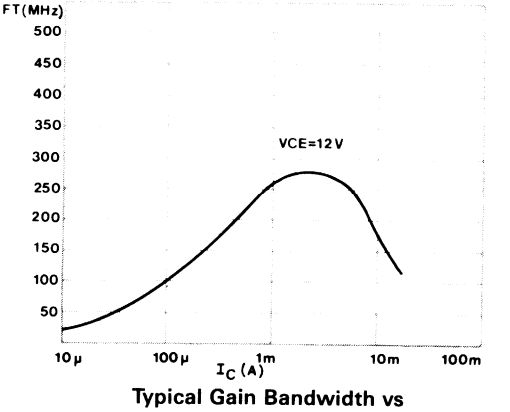
Saturation Voltage vs Emitter Current



Typical Saturation Voltage vs Forced HFE

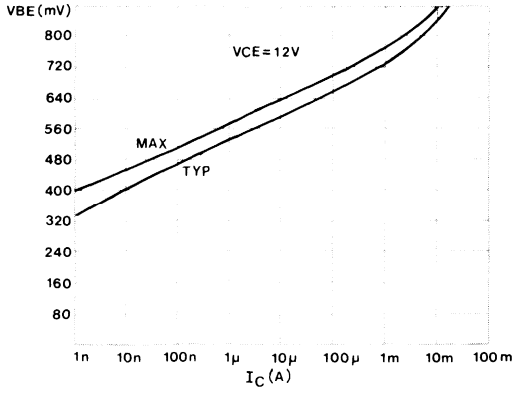


Typical Saturation Voltage vs Ambient Temperature

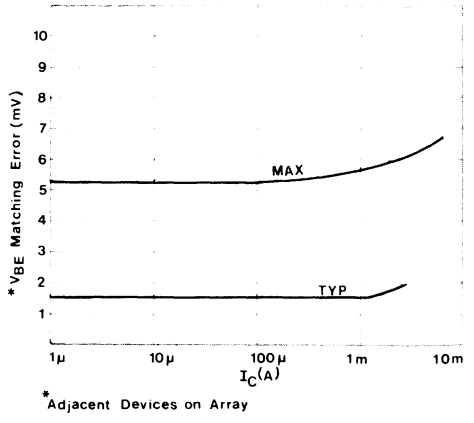


Typical Gain Bandwidth vs Collector Current

4-3



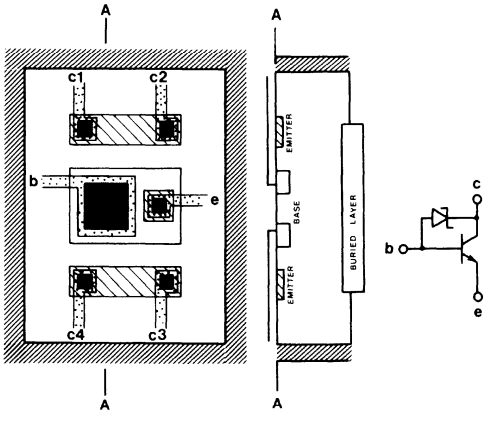
Base Emitter Voltage vs Collector Current



V_{BE} Matching Error

SCHOTTKY CLAMPED NPN

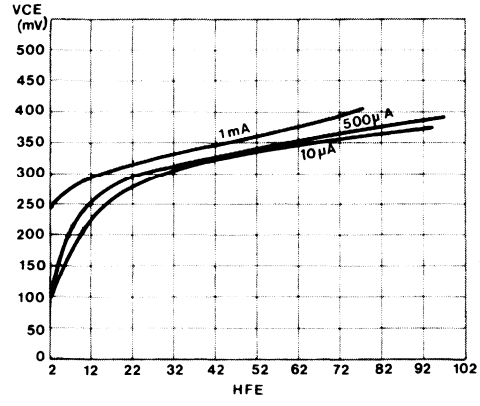
This npn transistor has an additional Schottky diode connected between its base and collector by allowingthe metal to contact the epitaxial layer through a hole in the base diffusion. This Schottky diode can prevent hard saturation when the cell is used as an npn transistor, or it may be accessed independently with the base and collector contacts. Since this transistor cell is not suitable in low saturation applications, the normal wrap-around collector has been replaced by two separate pick-ups which may still be used as low resistance cross-unders, with the resistance between the two collector pick-ups as approximately 150 Ω.



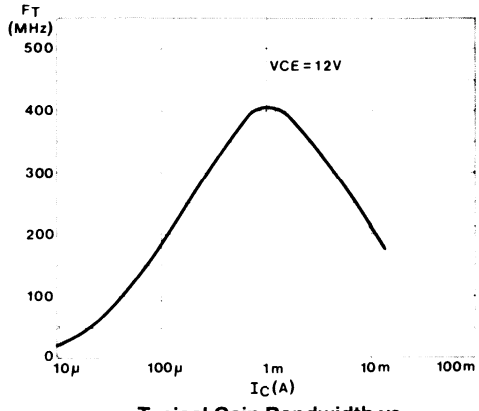
Schottky NPN Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
H_{FE}	I_C = 1 mA, V_{CE} = 12 V	80		320	
V_{BE}	I_C = 10 μA, V_{CE} = 12 V		600	640	mV
V_{BC}	I_C = -10 μA, I_B = 10 μA		410	450	mV
$V_{CE(SAT)}$	I_C = 10 μA, I_B = 1 μA	200	290		mV
BV_{CEO}	I_C = 20 μA, I_B = 0	20	27		V
BV_{EBO}	I_E = 20 μA, I_C = 0	6.5	7.5		V
I_{CEO}	V_{CE} = 12 V		200		pA
I_{CBO}	V_{CB} = 12 V		20		pA
V_A	I_B = 10 μA, V_{CE} = 5 V and 15 V	50	100		V
C_{OB}	f = 1 kHz, V_{CB} = 0		3.7		pF
f_T	I_C = 1 mA, V_{CE} = 12 V		400		MHz

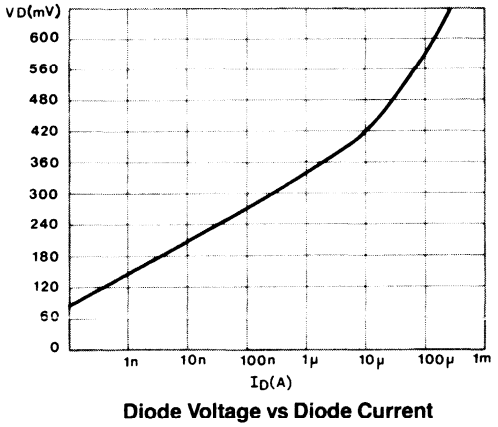
Schottky Graphs



Typical Saturation Voltage vs Forced HFE



Typical Gain Bandwidth vs Collector Current

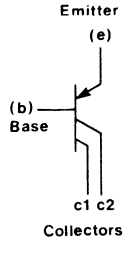


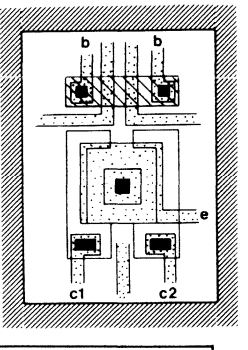
Diode Voltage vs Diode Current

Note: For characteristics not shown see section on Small Emitter NPN

SPLIT COLLECTOR PNP

The pnp transistors are of the lateral action construction with the collector split into two equal segments.
This structure may be used as a single pnp when both collectors are connected together. It may also be considered as two pnp transistors with common emitters and common bases. When considered as two transistors it can be used to implement current sources, current mirrors and area ratios on an integrated circuit.





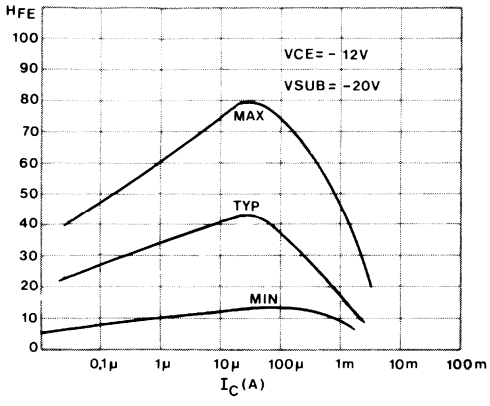
4-5

Split Collector PNP
(with both collectors connected together)

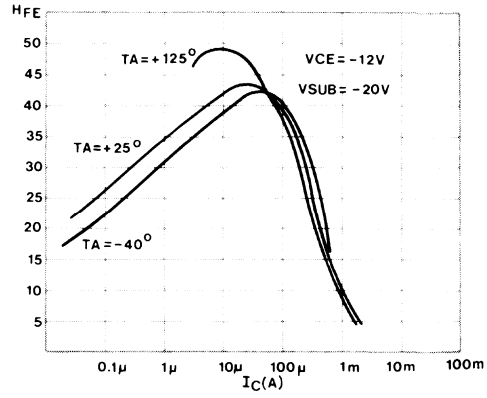
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
H_{FE}	I_C = 30 μA, V_{CE} = -12 V, V_{SUB} = -20 V	15	40		
V_{BE}	I_C = 10 μA, V_{CE} = -12 V, V_{SUB} = -20 V	540	600		mV
$V_{CE(SAT)}$	I_C = 100 μA, I_B = 50 μA, V_{SUB} = -20 V		90	120	mV
BV_{CEO}	I_C = 20 μA, I_B = 0	20	27		V
BV_{EBO}	I_E = 20 μA, I_C = 0	20	27		V
I_{CEO}	V_{CE} = -12 V		100		pA
I_{CBO}	V_{CB} = -12 V		5		pA
V_A	I_B = 10 μA, V_{CE} = -5 V and -15 V	30	42		V
C_{OB}	f = 1 kHz, V_{CB} = 0		0.96		pF
f_T	I_C = 100 μA, V_{CE} = -12 V, V_{SUB} = -20 V		3.5		MHz

ΔV_{BE} for adjacent devices 2mV typ (6mV max)

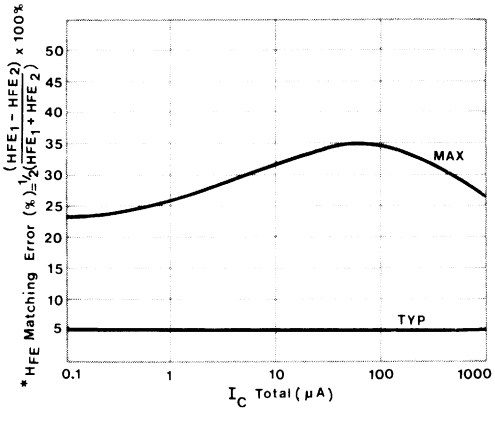
PNP Graphs



DC Current Gain vs Collector Current

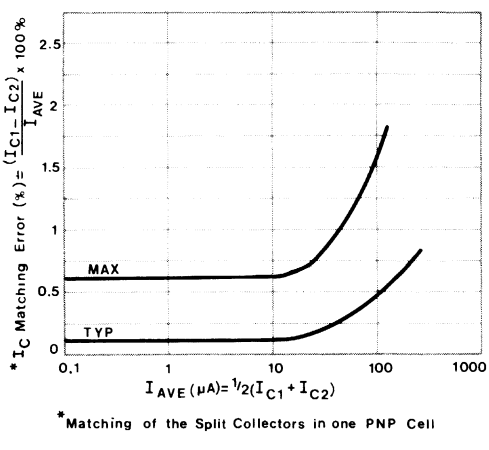


Typical DC Current Gain vs Collector Current over Temperature



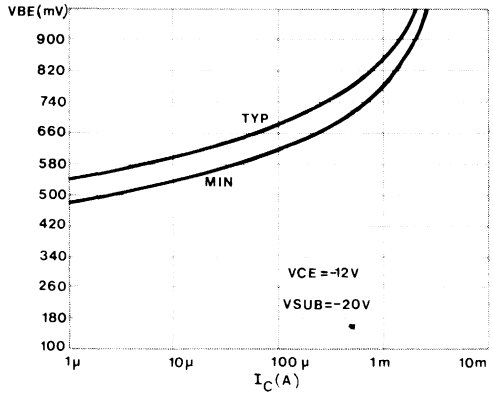
*Adjacent Devices on Array with both Collectors joined

HFE Matching Error

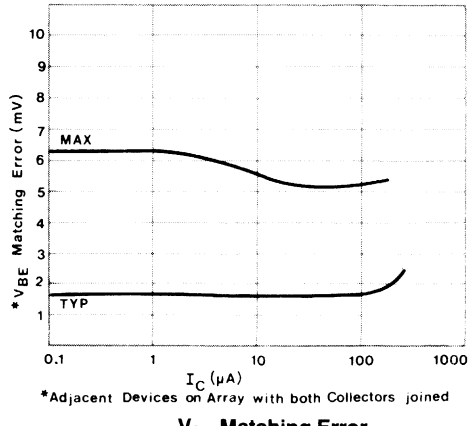


*Matching of the Split Collectors in one PNP Cell

Collector Current Matching (%)



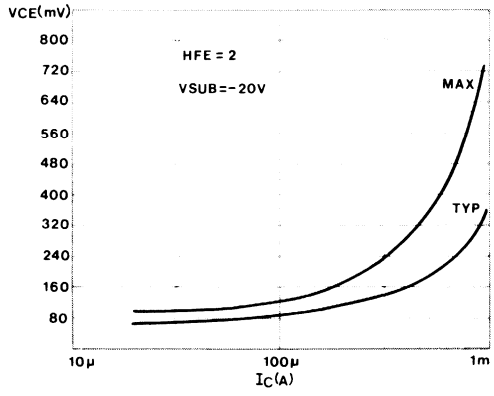
Base Emitter Voltage vs Collector Current



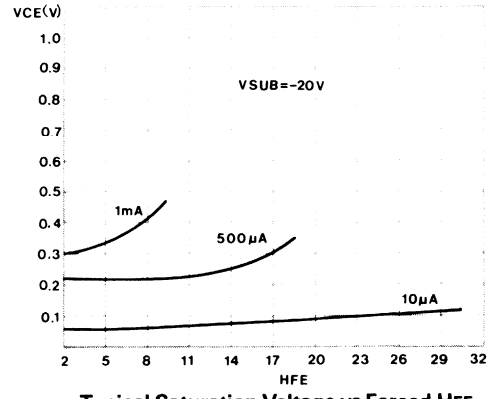
*Adjacent Devices on Array with both Collectors joined

VBE Matching Error

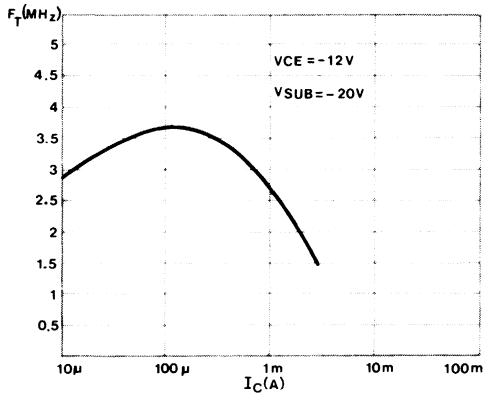
PNP Graphs (continued)



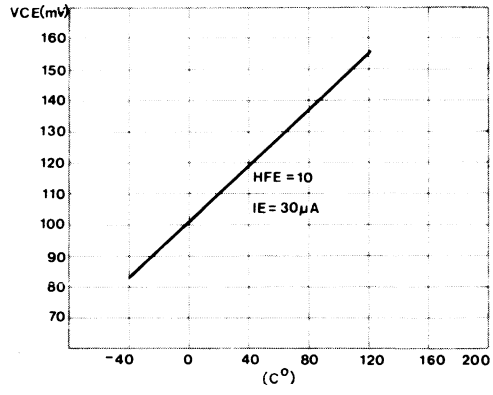
Saturation Voltage vs Emitter Current



Typical Saturation Voltage vs Forced HFE



Typical Gain Bandwidth vs Collector Current



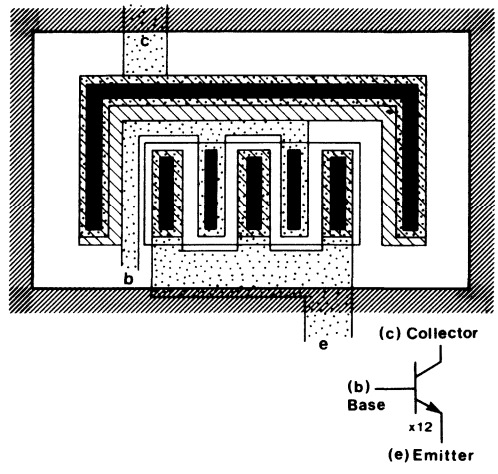
Saturation Voltage vs Ambient Temperature

4-7

LARGE NPN

This is approximately equivalent to 12 small npns connected in parallel. Since there are only two in the array, no provision has been made for cross-unders in this structure, although care has been taken to allow the base connection to be made from either side of the transistor. Note that each of these transistors can pass substantial current but the main limiting factor is probably the power being dissipated by the device. Here, the power is the product of the voltage across the transistor and the current in the collector, e.g. $P_d = V_{CE} \cdot I_C$.

This is one contribution to the overall power being dissipated on the die, which should be limited according to the chosen package.

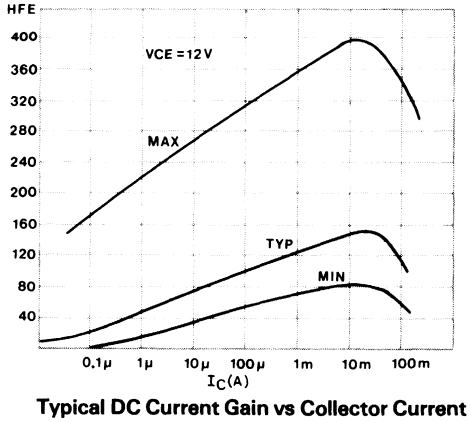


Large NPN Characteristics

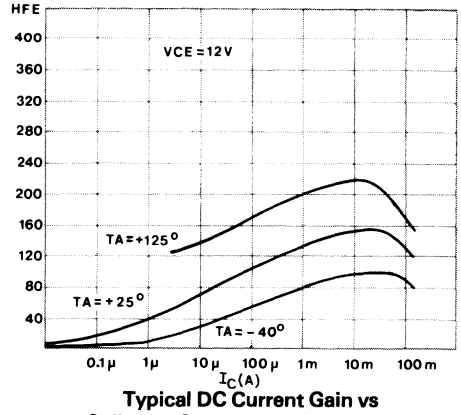
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
H_{FE}	I_C = 12 mA, V_{CE} = 12 V	80		400	
V_{BE}	I_C = 10 mA, V_{CE} = 12 V		790	850	mV
	I_C = 1 mA, V_{CE} = 12 V		680	740	mV
$V_{CE(SAT)}$	I_C = 1 mA, I_B = .1 mA		60	100	mV
	I_C = 10 mA, I_B = 1 mA		160	350	mV
BV_{CEO}	I_C = 20 μA, I_B = 0	20	27		V
BV_{EBO}	I_E = 20 μA, I_C = 0	6.5	7.5		V
I_{CEO}	V_{CE} = 12 V		15		pA
I_{CBO}	V_{CB} = 12 V		30		pA
V_A	I_B = 10 μA, V_{CE} = 5 V and 15 V	50	100		V
C_{OB}	f = 1 kHz, V_{CB} = 0		10.7		pF
f_T	I_C = 18 mA, V_{CE} = 12 V		350		MHz

1mV typ (5mV max)

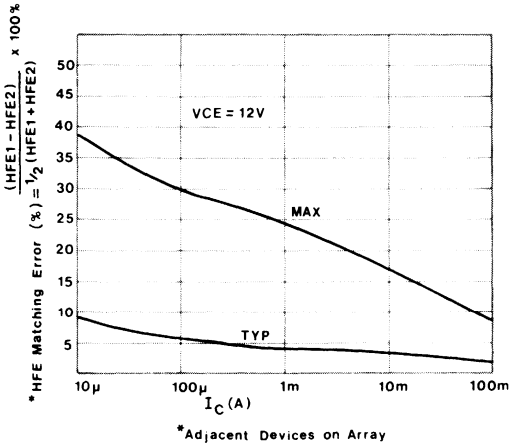
Large NPN Graphs



Typical DC Current Gain vs Collector Current

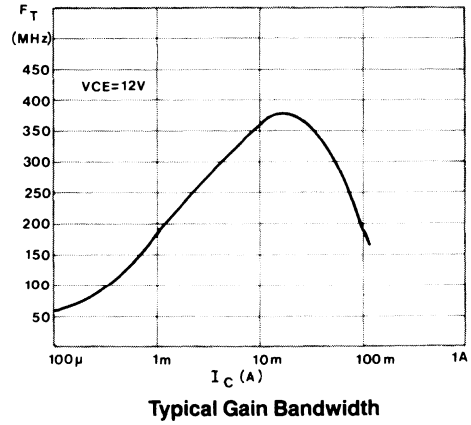


Typical DC Current Gain vs Collector Current over Temperature



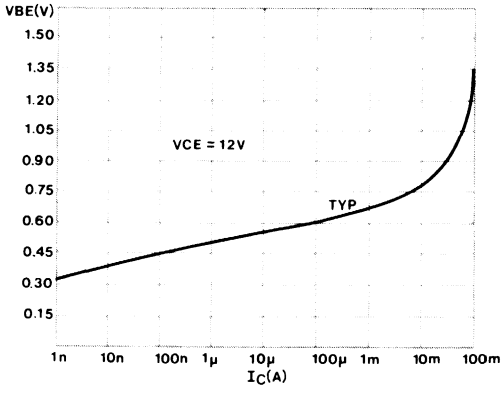
*Adjacent Devices on Array

H_{FE} Matching Error

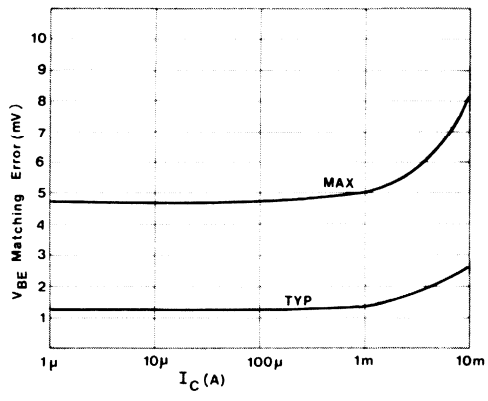


Typical Gain Bandwidth vs Collector Current

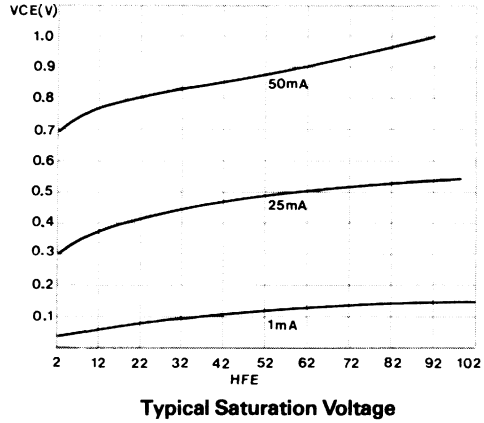
Large PNP Graphs



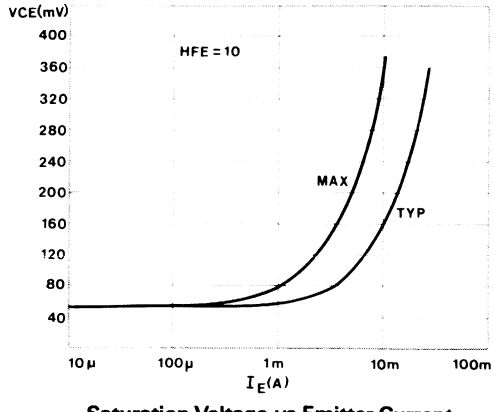
Base Emitter Voltage vs Collector Current



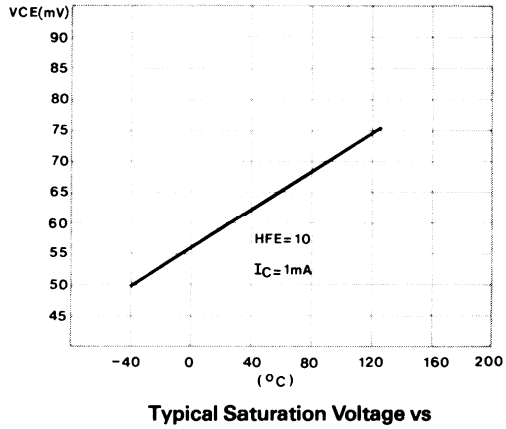
V_{BE} Matching Error



Typical Saturation Voltage vs Forced HFE



Saturation Voltage vs Emitter Current



Typical Saturation Voltage vs Ambient Temperature

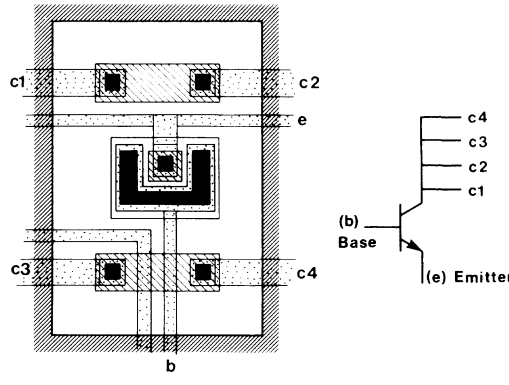
LOW NOISE NPN

Legend for component drawings

Metallization | Contact | Emitter | Base and Isolation | Base on Isolation in Zener Structure | Deep Collector Diffusion

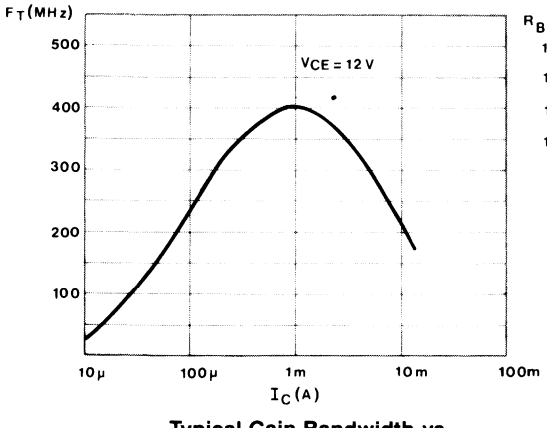
This device features a large base contact area which provides lower noise and better high frequency performance than the standard small npn.

Although intended primarily for the input stages of amplifiers, it may also be used for any standard small npn applications. The two collector pick-ups may be used as cross-unders if required, and in this respect the device is similar to the Schottky npn transistor.

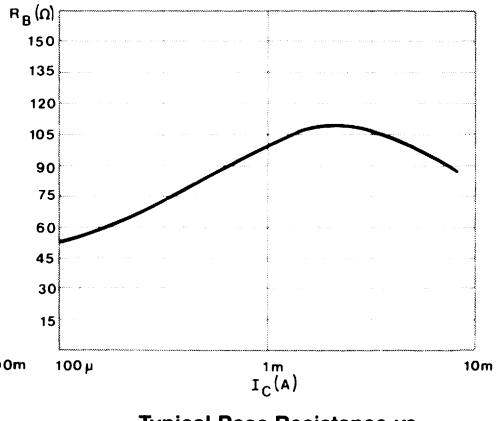


Low Noise NPN Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
H_{FE}	I_C = 1 mA, V_{CE} = 12 V	80		320	
V_{BE}	I_C = 10 μA, V_{CE} = 12 V		600	640	mV
$V_{CE(SAT)}$	I_C = 10 mA, I_B = 1 mA		270	400	mV
	I_C = 1 mA, I_B = 1 mA		100	200	mV
BV_{CEO}	I_C = 20 μA, I_B = 0	20	27		V
BV_{EBO}	I_E = 20 μA, I_C = 0	6.5	7.5		V
I_{CEO}	V_{CE} = 12 V		12		pA
I_{CBO}	V_{CB} = 12 V		6		pA
V_A	I_B = 10 μA, V_{CE} = 5 V and 15 V	50	100		V
C_{OB}	f = 1 kHz, V_{CB} = 0		3.7		pF
f_T	I_C = 3 mA, V_{CE} = 12 V		350		MHz

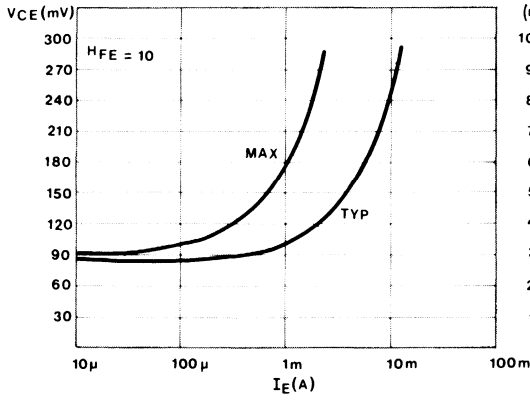


Typical Gain Bandwidth vs Collector Current

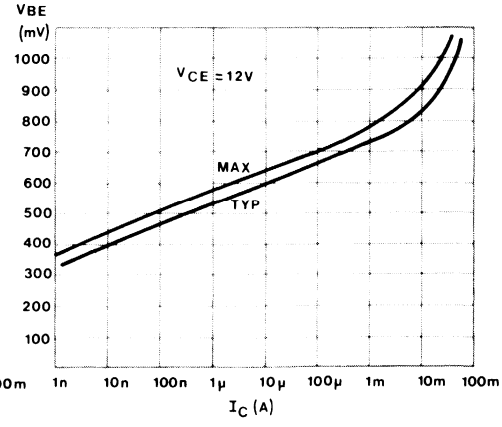


Typical Base Resistance vs Collector Current

Low Noise NPN Graphs (continued)



Saturation Voltage vs Emitter Current



Base Emitter Voltage vs Collector Current

Note: For characteristics not shown see section on Small Emitter NPN

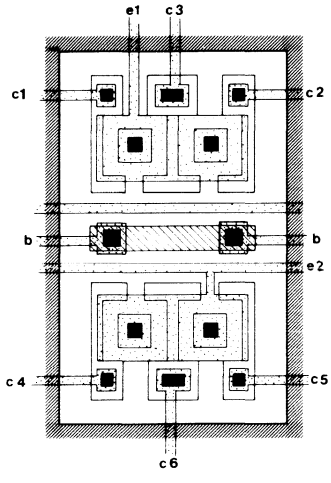
MULTIPLE COLLECTOR PNP

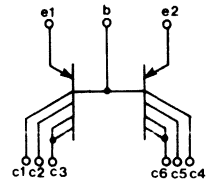
These pnp transistors are of the lateral action construction with the collector split in six segments.

Collectors c1, c2, c4 and c5 have the same effective "emitter area" as standard split collector pnp's. Collectors c3 and c6 are "double area".

The device can be used as a multiple current source or by connecting all collectors together as a pnp with better current handling, i.e. peak H_{FE} approx .- 120 μA.

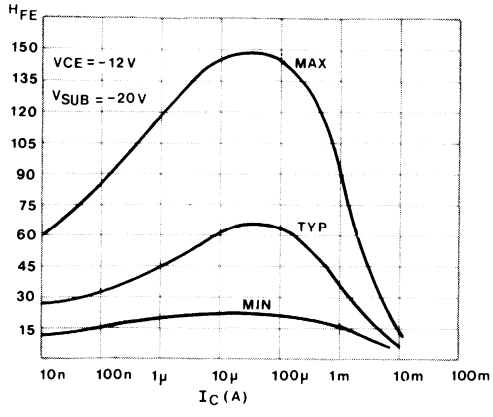
We suggest e1 and e2 be shorted together to prevent possible crosstalk between emitters. If c6 and c3 are considered as two single collectors in parallel, then the current matching performance of the collectors is as described by the collector current matching graph for the twin collector PNP.



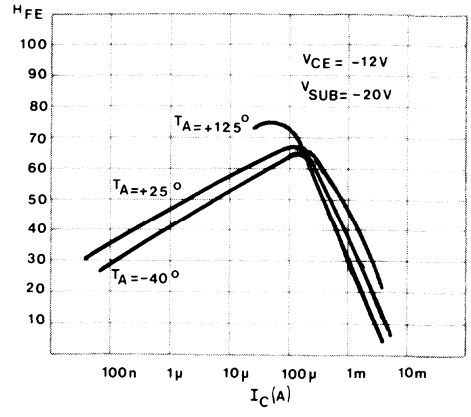


Multiple Collector PNP
(with all collectors connected together and emitters connected together)

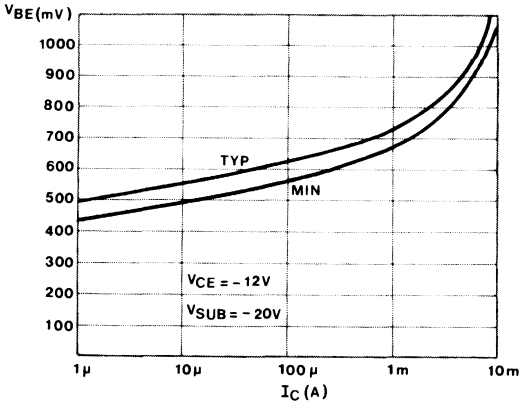
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
H_{FE}	I_C = 120 μA, V_{CE} = −12 V, V_{SUB} = −20 V	20	65		
V_{BE}	I_C = 40 μA, V_{CE} = −12 V, V_{SUB} = −20V	540	600		mV
$V_{CE(SAT)}$	I_C = 400 μA, I_B = 200 μA, V_{SUB} = −20 V		90	120	mV
BV_{CEO}	I_C = 20 μA, I_B = 0	20	27		V
BV_{EBO}	I_E = 20 μA, I_C = 0	20	27		V
I_{CEO}	V_{CE} = −12 V		400		pA
I_{CBO}	V_{CB} = −12 V		20		pA
V_A	I_B = 10 μA, V_{CE} = −5 V and −15 V	30	70		V
C_{OB}	f = 1 kHz, V_{CB} = 0		3.8		pF
f_T	I_C = 400 μA, V_{CE} = −12 V, V_{SUB} = −20 V		3.5		MHz



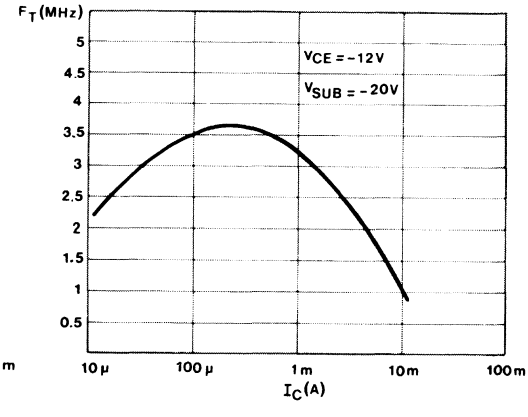
DC Current Gain vs Collector Current



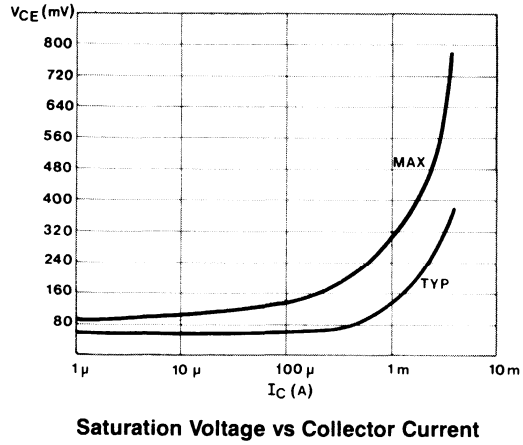
Typical DC Current Gain vs Collector Current over Temperature



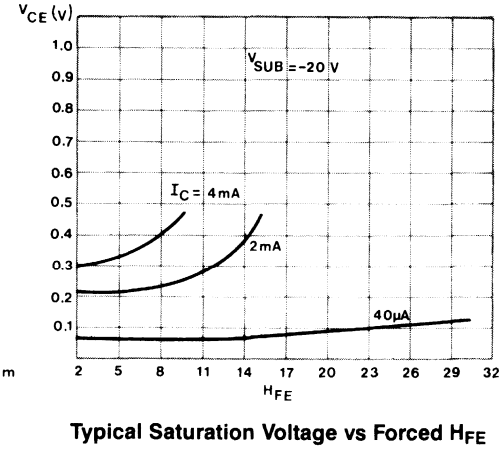
Base Emitter Voltage vs Collector Current



Typical Gain Bandwidth vs Collector Current

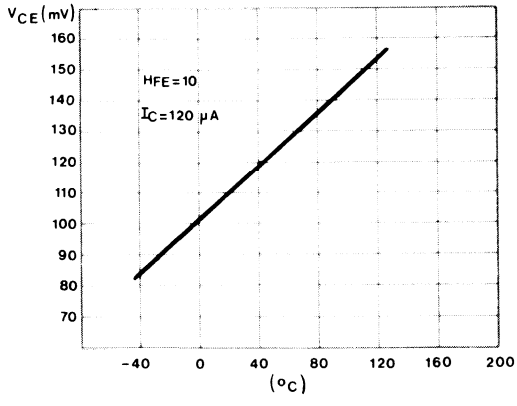


Saturation Voltage vs Collector Current



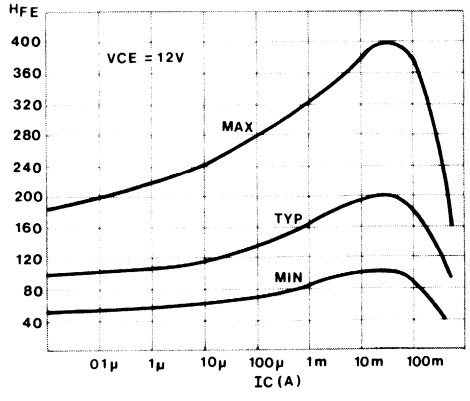
Typical Saturation Voltage vs Forced H_{FE}

Multiple Collector PNP Graphs (continued)



Typical Saturation Voltage vs Ambient Temperature

Power NPN Graph



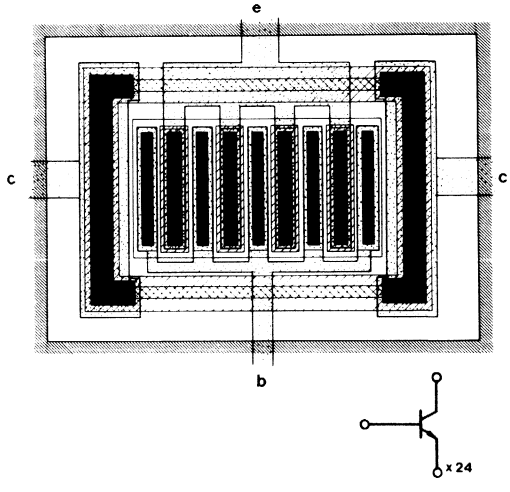
DC Current Gain vs Collector Current

POWER NPN

This transistor has approximately twice (2x) the emitter area of the large npn device on the LA200 series arrays and twenty four times (24x) the emitter area of the small npn; hence' a correspondingly higher current capability (I_C max. = 300 mA). In addition to being physically larger, the device has a number of extra features which offer an enhanced performance over the LA200 series large npn.

These features are:

- Four separate emitter structures to provide improved gain at high collector currents.
- Five base contacts to reduce the VBE for high base currents and improve switching speed.
- An all-around deep collector diffusion to ensure a low saturation voltage in switching applications.



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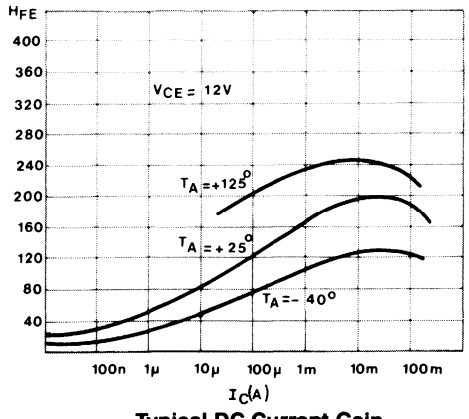
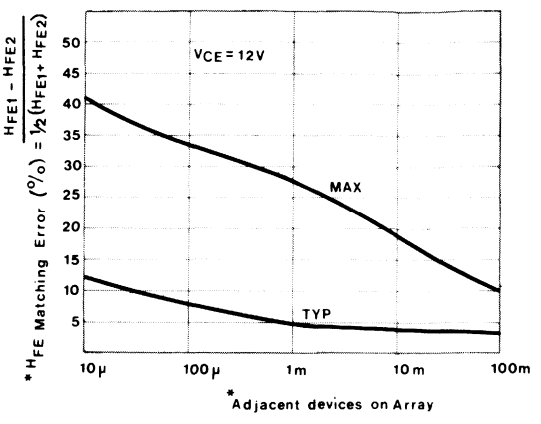
Power NPN Characteristics

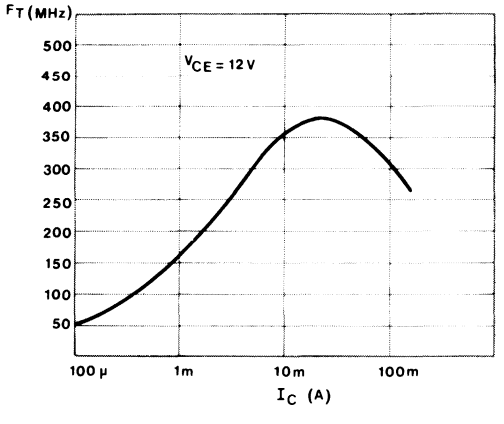
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
H_{FE}	I_C = 20 mA, V_{CE} = 12 V	100		400	
V_{BE}	I_C = 10 mA, V_{CE} = 12 V		660		mV
	I_C = 1 mA, V_{CE} = 12 V		595		mV
$V_{CE(SAT)}$	I_C = 1 mA, I_B = 1 mA		15	26	mV
	I_C = 10 mA, I_B = 1 mA		50	100	mV
BV_{CEO}	I_C = 20 μA, I_B = 0	20	27		V
BV_{EBO}	I_E = 20 μA, I_C = 0	6.5	7.5		V
I_{CEO}	V_{CE} = 12 V		50		pA
I_{CBO}	V_{CB} = 12 V		25		pA
V_A	I_B = 10 μA, V_{CE} = 5 V and 15 V	50	100		V
C_{OB}	f = 1 kHz, V_{CB} = 0		14		pF
f_T	I_C = 36 mA, V_{CE} = 12 V		350		MHz



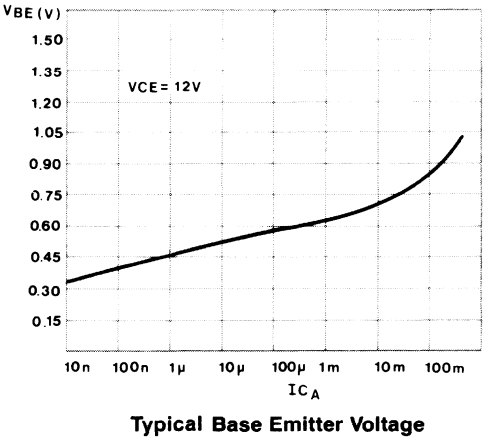
Typical DC Current Gain vs Collector Current over Temperature



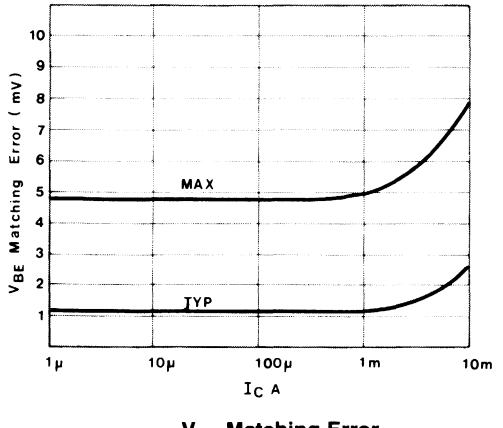
H_{FE} Matching Error



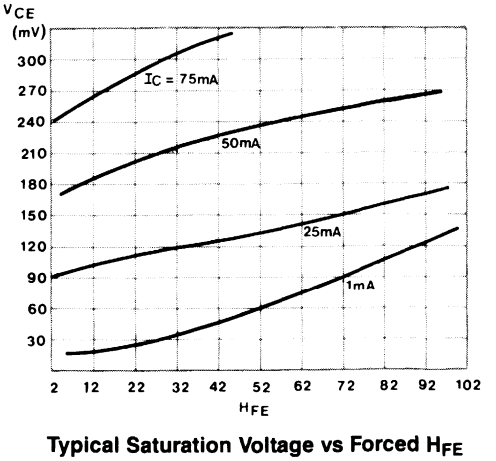
Typical Gain Bandwidth vs Collector Current



Typical Base Emitter Voltage vs Collector Current

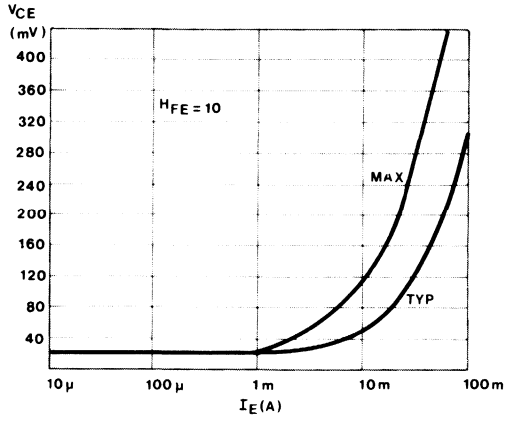


V_{BE} Matching Error



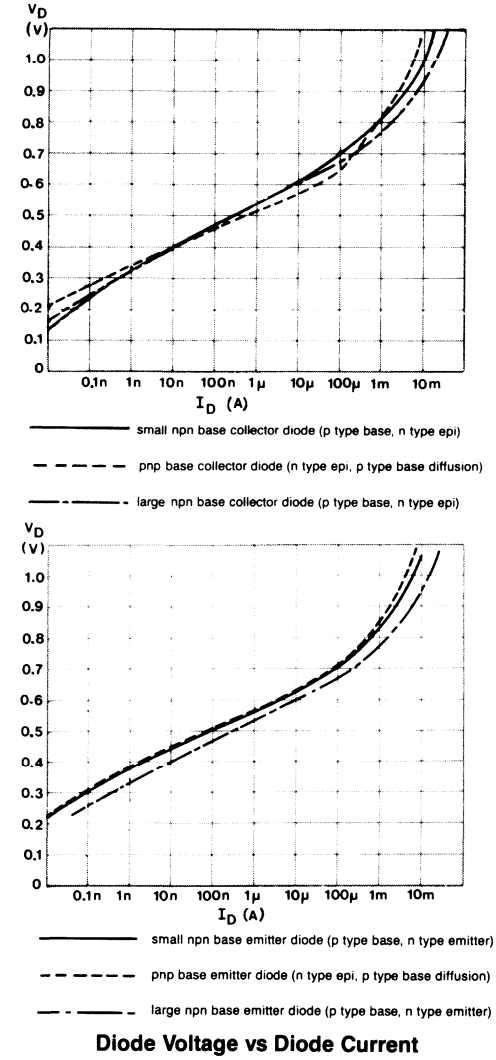
Typical Saturation Voltage vs Forced H_{FE}

Power NPN Graph (continued)



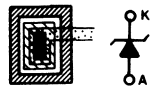
Saturation Voltage vs Emitter Current

Zener Diode Graphs



Diode Voltage vs Diode Current

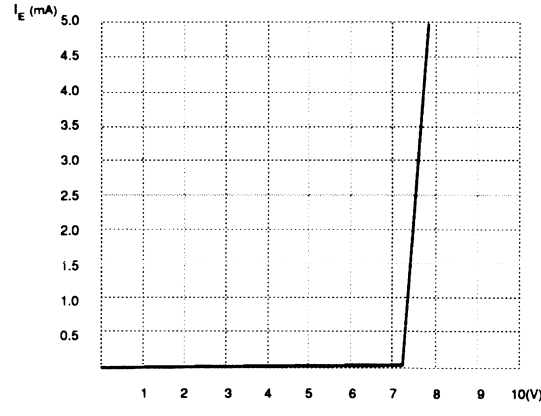
ZENER DIODE



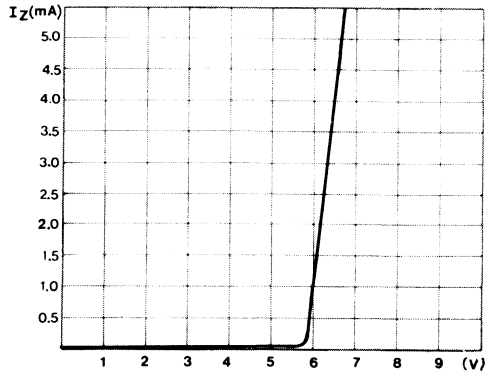
Anode to substrate

This is a generally accepted term for any p-n junction used in thereverse breakdown mode. The voltage at which the reverse biased junction starts to pass significant current is a function of the doping levels of the p-type and the n-type semi-conductor in question. Any number of components on the array may be used in such a way that it will break down a junction and pass current, however, the voltage at which this happens directly affects the temperature coefficient of the resulting reference voltage. The zener diode which is specifically provided as a voltage reference has a breakdown of approximately 5.8 V with respect to substrate. The sandwich capacitors may be used in this mode with a zener diode breakdown of approximately 5.8 V ±0.5 V across the capacitor contacts and without respect to substrate. The temperature coefficient of breakdown voltage is +200 ppm/°C.

Any npn transistor may be used as a zener reference by reverse biasing the base-emitter junction which will break down at approximately 7.5 V with a slope resistance of 100 Ω.



Breakdown Voltage of Reverse Biased Base – Emitter Junction of Small NPN

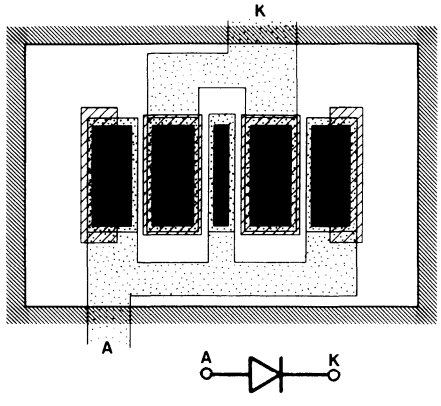


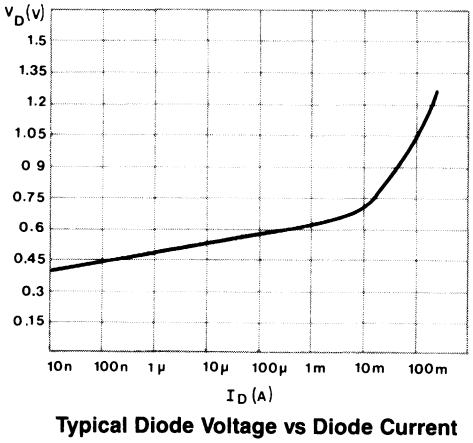
Zener Diode Breakdown Characteristics

DIODES

Large Diode

Two large diodes are provided on the LA251 ans LA252 arrays for applications where high forward current is required. The reverse breakdown characteristic is similar to that of an npn base-emitter junction.





Typical Diode Voltage vs Diode Current

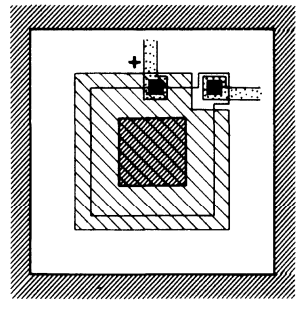
Implementing Diodes using Array Transistors

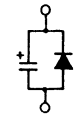
		Diode Voltage at 10 μA	Reverse Breakdown Voltage
Small/Low noise npn	base - emitter	0.6	7.5 V
Small/Low noise npn	base - collector	0.6	>20 V
Small/Multiple pnp	base - emitter	0.6	>20 V
Schottky npn	base - collector	0.4	>20 V
Large/Power npn	base - emitter	0.6	7.5 V
	base - collector	0.6	>20 V

CAPACITORS

The three large area capacitors which are in the corners of the die are junction capacitors with an emitter (diffusion) on base (diffusion) on isolation construction which is often referred to as a *sandwich capacitor.* This type of capacitor has an equivalent circuit as shown: Thus the forward bias voltage is approximately 0.6 V and the reverse bias breakdown voltage is that of the zener diode at 5.8 V (approximately). The nominal value is 75 pF.

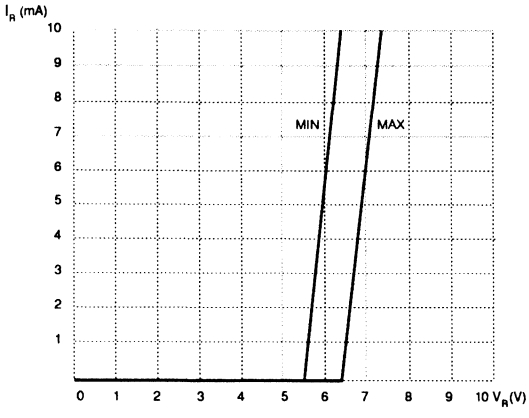
In addition, the intrinsic capacitance of any of the structures may be used. In particular, the reverse biased collector to base junction of the npn structures may be used at any voltage up to 20 V.



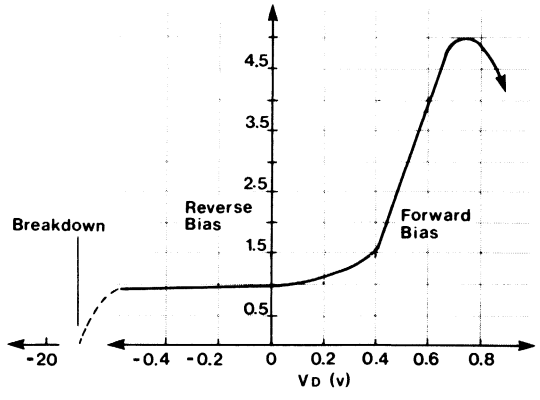


Capacitors				
TYPE	NOMINAL VALUE	TOLERANCE OF NOMINAL	ZENER BREAKDOWN VOLTAGE	TEMPERATURE COEFFICIENT OF BREAKDOWN VOLTAGE
Sandwich	*75 pF	± 20%	5.8 V ± 0.5 V	+ 200 ppm/°C
Collector-Base Junction of small npn	0.4pF	± 20%	> 20 V	Do not use in breakdown mode
Collector-Base Junction of large npn	4.7 pF	± 20%	> 20 V	Do not use in breakdown mode
Emitter-Base Junction of small npn	0.7pF	± 20%	7.5 ± 1 V	+ 500 ppm/°C
Emitter-Base Junction of large npn	5.7 pF	± 20%	7.5 ± 1 V	+ 500 ppm/°C

* 56 pF on LA204 array



Reverse Breakdown Characteristic of Sandwich Capacitor

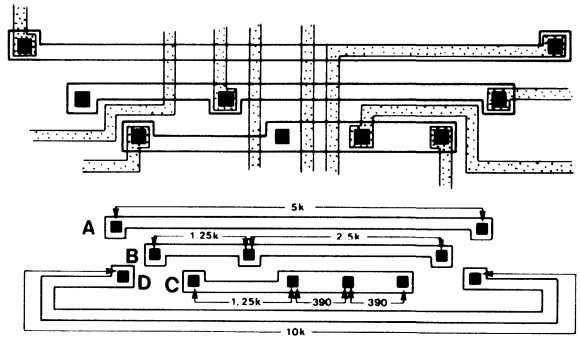


Normalized Capacitance (with respect to C_{jO}) for a PN Junction Capacitor

RESISTORS

All the resistors in the common land are formed during the base diffusion for the npn transistors and are termed "base resistors".

They have nominal values of 10 k (250 series only), 5 k, 2.5 k, 1.25 k and 390 Ω as shown on the diagram of a resistor grouping but their absolute values are dependent on the base diffusion sheet resistivity and so may have a variation of ±25%. However, a ratio of one resistor to another is considerably better and for identical resistors lying side by side on the die the matching tolerance will be ±4% at the three sigma points.



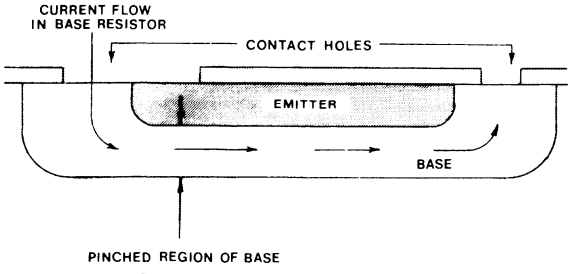
Notes.
1. Resistor values are shown in ohms and are the resistance between adjacent contacts.
2. In the above combination of narrow and wide resistors matching is worse than for like types.

Resistors

TYPE	NOMINAL VALUE	ABSOLUTE TOLERANCE	MATCHING TOLERANCE	TEMPERATURE COEFFICIENT
A	5 k	± 25%	± 4%	+ 2000 ppm/°C
B	2.5 k 1.25 k	± 25%	± 4%	+ 2000 ppm/°C
C	1.25 k	± 25%		+ 2000 ppm/°C
	390		± 2%	
	390		± 2%	
D	10 k	± 25%	± 4%	+ 2000 ppm/°C
Pinch	40 k	+ 100% − 50%	± 15%	+ 5000 ppm/°C

PINCH RESISTORS

A pinch resistor is formed by putting emitter diffusion on top of a base resistor so that theeffective thickness of the resistor is greatly reduced. In this way, the resistance may be increased by a factor of ten.



Sectional View of Pinch Resistors

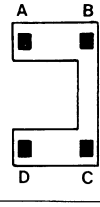
By applying a bias voltage to the emitter region, the associated depletion region further pinches off the base resistor until the reverse breakdown voltage is reached. Since this is the same as a reverse biased base emitter junction of an npn transistor, the pinch resistor will break down at approximately 7.5 volt. A full description of the voltage dependence of the resistor as the bias voltage is applied is shown on the graph Pinch Resistance vs Applied Voltage.

CROSS - UNDERS

Standard Small NPN

The resistance between the four collector contacts is distributive, hence it is best described by a matrix.
e.g. R_{AC} = 20 Ω

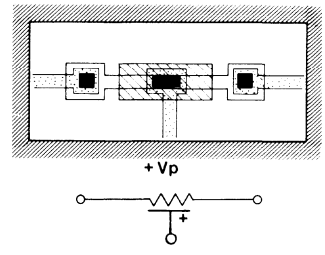
Ω	B	C	D
A	7	20	23
B	-	16	20
C	16	-	7



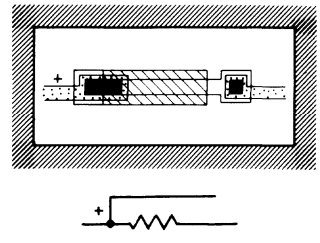
Additional Data for Emitter Diffusion Resistors (cross - unders)		
ABSOLUTE TOLERANCE	MATCHING TOLERANCE	TEMPERATURE COEFFICIENT
± 50%	± 5%	+ 600 ppm/°C

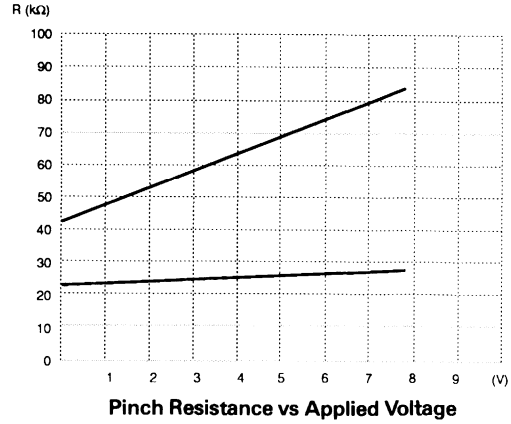
LA250 SERIES PINCH RESISTOR

This is essentially the same device as on the LA200 series, except a separate contact is provided for applying the bias voltage, allowing greater flexibility in layouts. As always, the bias contact should be connected to the most positive end of the resistor.



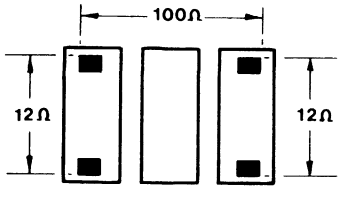
LA250 Small Series Pinch Resistor



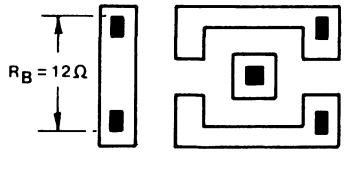


Pinch Resistance vs Applied Voltage

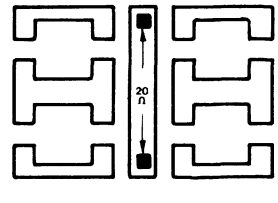
SCHOTTKY/LOW NOISE NPN

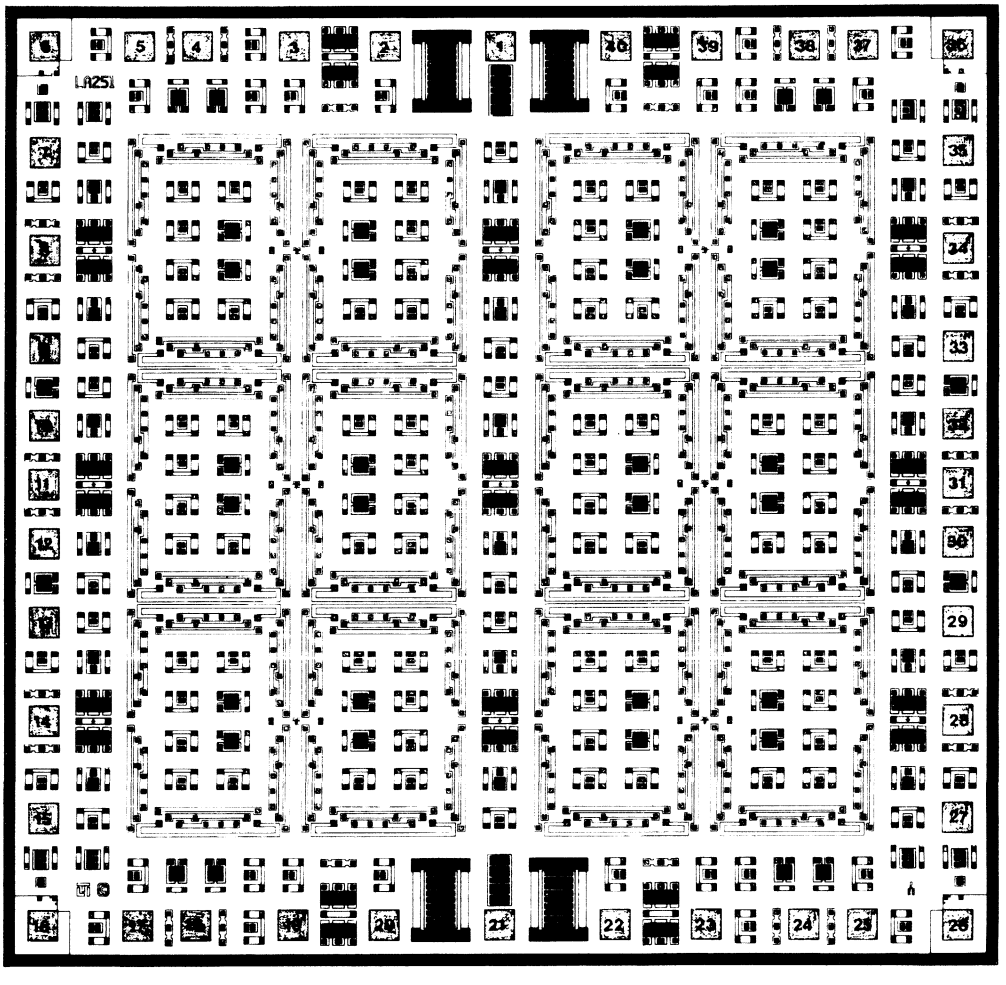


SPLIT COLLECTOR PNP BASE



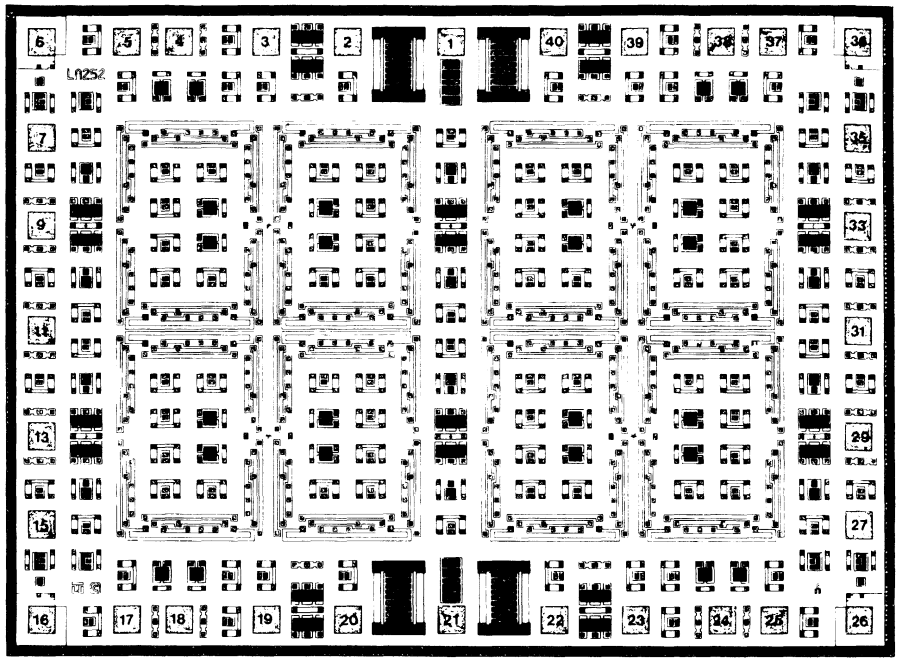
MULTIPLE COLLECTOR PNP BASE





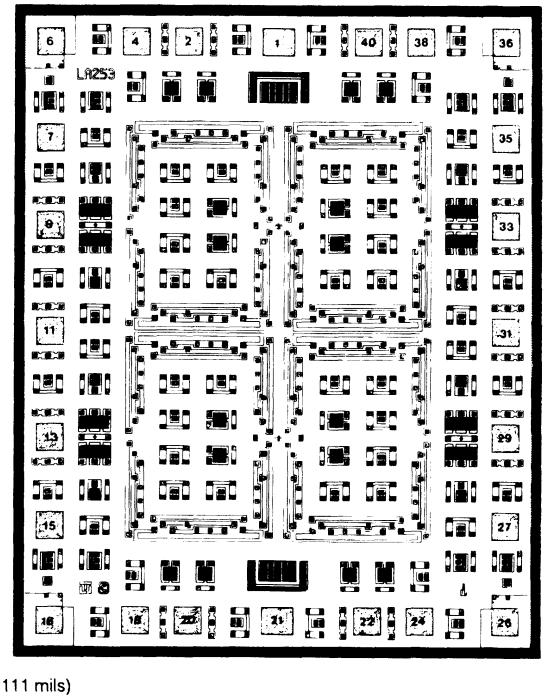
LA251 (SIZE 150 x 144 mils)
Maximum number of bonding pads available - 40

MODULA LA250 SERIES ARRAY LAYOUT



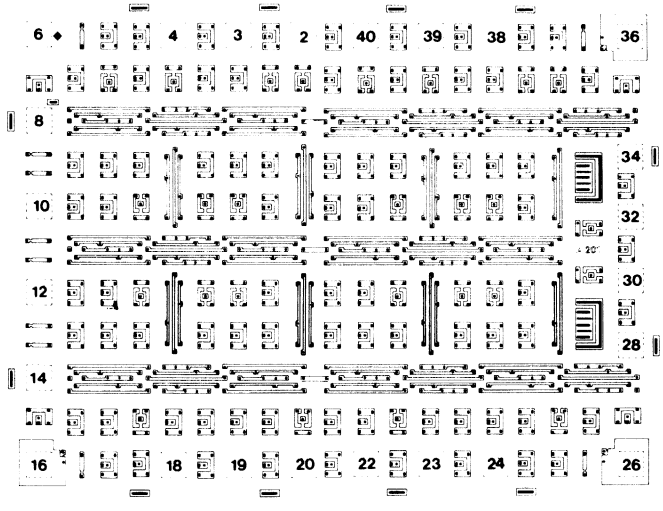
LA252 (SIZE 151 x 111 mils)
Maximum number of bonding pads available - 32

MODULA LA250 SERIES ARRAY LAYOUT



LA253 (SIZE 92 x 111 mils)
Maximum number of bonding pads available - 24

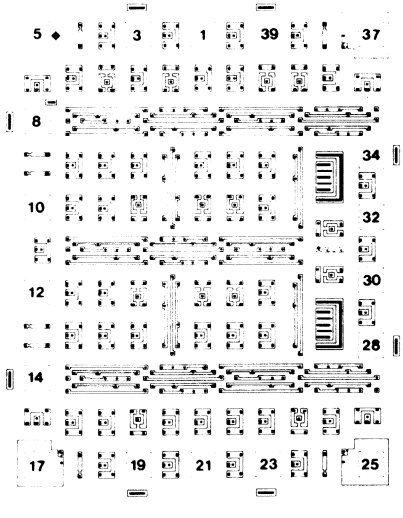
MODULA LA250 SERIES ARRAY LAYOUT



LA201 (SIZE 127 x 94 mils)

Maximum number of bonding pads available - 24

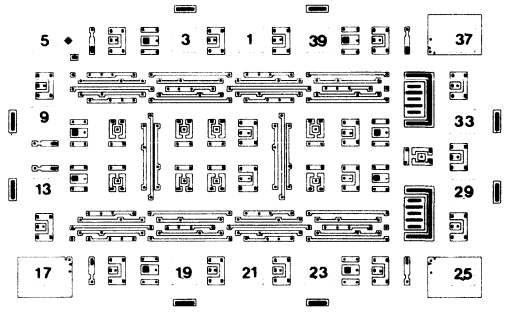
LA200 SERIES ARRAY LAYOUT



LA202 (SIZE 78 x 94 mils)

Maximum number of bonding pads available - 18

LA200 SERIES ARRAY LAYOUT



LA204 (SIZE 56 x 91 mils)

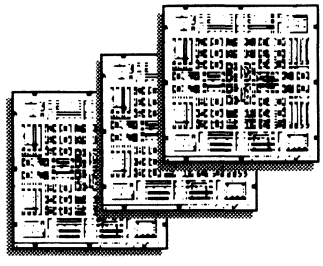
Maximum number of bonding pads available - 18

LA200 SERIES ARRAY LAYOUT

GENNUM CORPORATION

Information Note

'The Preferred Source for Analog ASICs'



RF Analog Array
GA911

TILE BASED ARRAY — GA911

Features:	**High Speed Process** **2.5 GHz f_T**	**Low Power Capability** **1 V operation**
Flexible Array Size	**1100 NPNs** **460 PNPs** **76 Bonding pads**	**PC-based Design Tools**

Fast Turnaround on Protochips 1 - 2 weeks

Document No. 510 - 95 - 1

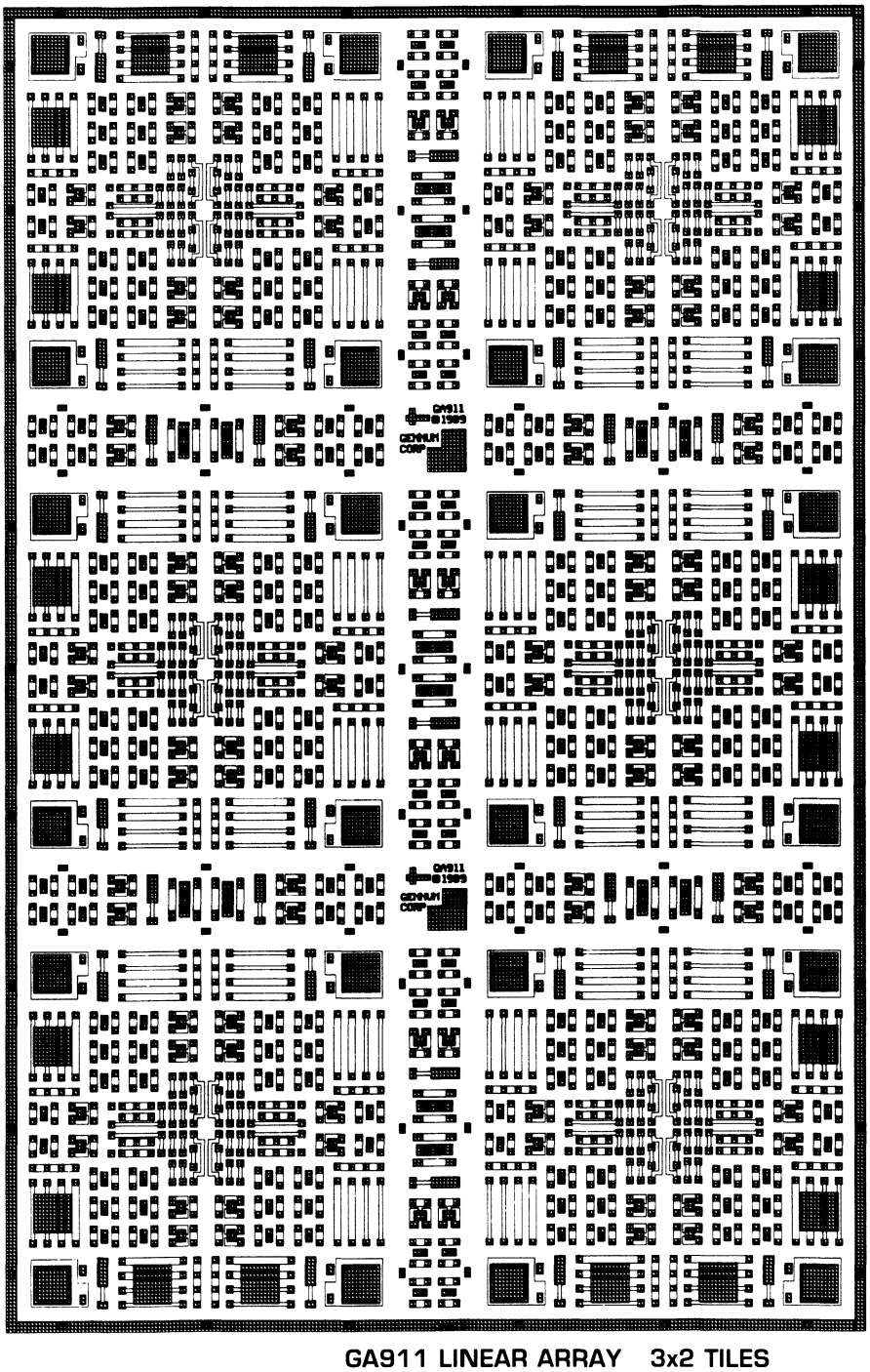
GENNUM CORPORATION P.O. Box 489, Stn A, Burlington, Ontario, Canada L7R 3Y3 tel.(416) 632-2996 fax:(416) 632-2055 telex: 061-8525
JAPAN BRANCH: 301 Aoba Building, 3-6-2, Minato-ku, Tokyo 108, Japan tel. (03) 441-2096 fax: (03) 448-8991

COMPONENT CHARACTERISTICS

Device Type	Parameter	Condition	Min	Typ	Max	Units
Small NPN	H_{FE}	I_C = 100 µA, V_{CE} = 1 V	-	130	-	
	B V_{CEO}		17	-	-	V
	B V_{EBO}		4	-	-	V
	B V_{CBO}		30	-	-	V
	f_T	I_C = 0.5 mA, V_{CE} = 1 V	-	2.5	-	GHz
Lateral PNP	H_{FE}	I_C = 100 µA, V_{CE} = 1 V	-	50	-	
	B V_{CBO}		20	-	-	V
	f_T	I_C = 15 µA	-	10	-	MHz
(N+ P-)Junction Capacitors	C_J	V_R = 2.5 V	-	6	-	pF
	V_R		4.5	-	-	V
Pinch Resistors	R_P		45	90	180	kΩ

SEMICUSTOM ARRAY - GA911 (15 VOLTS MAX)

	1x1	1x2	2x2	2x3	3x3	3x4	4x4	4x5	5x5
Active Components									
Small NPN (1x)	28	64	144	224	348	472	640	808	1020
Large NPN (18x)	-	2	8	14	24	34	48	62	80
Lateral PNP -split collectors	12	28	64	100	156	212	288	364	460
Junction Cap. / Vertical PNP	-	-	4	8	16	24	36	48	64
Passive Components									
Pinch Resistors (90 kΩ)	4	10	24	38	60	82	112	142	180
Diffused Resistors (ohms)	36 87 K	88 274 K	208 749K	328 1.22M	516 1.98M	704 2.75M	960 3.79M	1216 4.84M	1540 6.18M
Bonding Pads									
- High Freq.	8	12	16	20	24	28	32	36	40
- Low Freq.	4	8	12	16	20	24	28	32	36
Total	10	20	28	36	44	52	60	68	76
Chip Size (mils)	50x50	50x100	100x100	100x150	150x150	150x200	200x200	200x250	250x250



GA911 LINEAR ARRAY 3x2 TILES

Maximum number of tiles to an array is 5x5, minimum is 1x1.

HEARING INSTRUMENT PRODUCTS

For further information, technical data and application sheets, please contact the Hearing Instrument Products Department.

Availability should be confirmed with Gennum.

Some of these products are in the development stage and are subject to change without notice.

PART NO.	DESCRIPTION	PACKAGING
CLASS A AMPLIFIERS		
LC505	High gain class A amplifier	MINI 6
LD505	Class A amplifier with microphone decoupling resistor	MINI 8
LE507	Three transistor class A amplifier with 20 kHz frequency response; additional access pins supplied for design flexibility.	PLID 8, MICRO 8
LC508	Three inverting gain blocks, any two of which can be DC coupled. Third block is configured as a class A output stage. Feedback volume control gives >40dB range.	MINI10, PLID 10 MICRO 10, SLT 10
LP508	Two inverting gain blocks requiring only one external capacitor; gain blocks may be DC coupled. Second block is configuired as a class A output stage.	MINI 8 , PLID 8 MICRO 8, SLT 8
GC509	Three inverting gain blocks, any 2 of which can be DC coupled, third is class A output. Feedback volume control gives >40dB range. As LC508 with lower quiescent current.	MINI 10, PLID 10 MICRO 10, SLT 10
GP509	Two inverting gain blocks requires only one external capacitor; gain blocks may be DC coupled. Second block is class A output. As LP508 with lower quiescent current.	MINI 8, PLID 8 MICRO 8, SLT 8
CLASS A COMPRESSION AMPLIFIERS		
LD511	Low voltage monolithic AGC with adjustable attack and release time (fixed ratio); low transient during AGC; on-chip voltage regulator.	MINI 10, PLID 10 MICRO 10, SLT 10
LD512	Low parts, input AGC with class A output stage.	MICRO 8, PLID 8 SLT 8
CLASS A PEAK CLIPPING AMPLIFIERS		
LS505	Class A amplifier with microphone decoupling resistor and Schottky diodes in a feedback configuration for symmetrical peak clipping.	MINI 8, PLID 8 MICRO 8, SLT 8
LT505	Low current amplifier with on-chip Schottky diodes in a shunt configuration across the load, for symmetrical peak clipping.	MINI 8, PLID 8 MICRO 8, SLT 8
LS509	Contains two inverting preamps, a microphone decoupling resistor and an output stage with Schottky diodes for symmetrical peak clipping.	MINI 10, PLID 10 MICRO10
GK509	Two DC coupled, low noise inverting gain blocks with Schottky diode limiting in a feedback configuration. Second block is configured as a class A output stage.	MINI 8, PLID 8 MICRO 8, SLT 8

CLASS B AMPLIFIERS			MIN. LOAD (Ω)	MAX. CURRENT DRIVE (mA)
LC549	Single input amplifier with class B output stage; low voltage operation; low distortion; low power consumption.	MINI 8, PLID 8 MICRO 8	110	35
LD549	Selected LC549s for high output current	MINI 8, PLID 8 MICRO 8	110	~50
LV549	Selected LC549s for low to medium output current requirements.	MINI 8	110	~25
LC550	Low voltage, monolithic amplifier, combining a preamp and a medium power output stage.	MINI 10, PLID 10 MICRO 10, SLT 10	1000	11
LC551	High power output stage with gain from 0 to 48 dB; negligible start-up time; requires only 3 external capacitors.	MICRO10, PLID 10	110	50
GS551	High power class B output stage capable of driving low impedance loads; minimal start-up time; requires only 3 external capacitors.	MICRO10, PLID 10 SLT 10	68	50
LC552	Class A preamp with class B output stage; high gain; high power with low parts count.	DIP 14, MINI 14	110	50

PART NO.	APPLICATION	FREQ. (Hz)	OPERATING VOLTAGE (V)	GAIN (dB)	CURRENT CONSUMPT. (mA)	ACOUSTIC GAIN RANGE (dB)
LC505	low power hearing aids, microphone amplifiers, stethoscopes, communication helmets	100 - 5K	1 - 1.6	71	I_A = 0.2 I_T = 0.2 - 1.5	up to 48
LD505	low power hearing aids, microphone amplifiers, stethoscopes, communication helmets	100 - 5K	1 - 1.6	71	I_A = 0.2 I_T = 0.2 - 1.5	up to 48
LE507	hearing aids, filters and microphone preamps	200 - 20K	1 - 3	76 open 30 closed	I_Q = 1.3	output stage only
LC508	medium power high gain ITE and BTE aids, active filters and multi-channel systems	100 - 50K	1 - 5	73	I_A = 0.245 I_T = 0.275 - 1.3	up to 48
LP508	low power ITE and minimum parts count canal aids	100 - 50K	1 - 5	61	I_A = 0.195 I_T = 0.210 - 1.3	up to 35
GC509	medium power high gain ITE and BTE aids, active filters and multi-channel systems	100 - 50K	1 - 5	73	I_A = 0.145 I_T = 0.275 - 1	up to 48
GP509	low power ITE and minimum parts count canal aids	100 - 50K	1 - 5	61	I_A = 0.105 I_T = 0.300 - 1	up to 35
LD511	low and medium power compression aids microphone amplifiers, electronic stethoscopes, miniature tape recorders	300 - 6K	1.1 - 2.4	64	I_A = 0.4 I_T = 1.6	up to 50
LD512	low and medium power; medium gain ITE and canal aids	100 - 20K	1.1 - 5	57	I_A = 0.20 I_T = 1.0 max.	up to 39
LS505	low power BTE and ITE aids, microphone amplifiers, communication helmets	100 - 5K	1 - 1.6	72	I_A = 0.21 I_T = 1.5	up to 48
LT505	ITE and canal hearing aids where current consumption is critical	150 - 8K	1 - 1.6	74	I_A = 0.05 I_T = 0.2	up to 48
LS509	medium gain ITE/ITC hearing aids with output limiting	100 - 50K	1 - 5	73	I_A = 0.14 I_T = 0.23 - 1	up to 48
GK509	medium gain and low current hearing aids	100 - 50K	1 - 5	61	I_A = 0.10 I_T = 0.24 - 1	up to 35
LC549	hearing aids or general low voltage operation	50 - 20K	1 - 1.6	40	I_Q = 0.5	up to 80*
LD549	high power amplifiers for driving low impedance receivers	50 - 20K	1 - 1.6	40	I_Q = 0.5	up to 80*
LV549	medium to high power amplifiers for use when increased stability is required	50 - 20K	1 - 1.6	40	I_Q = 0.5	up to 80*
LC550	medium power BTE and ITE hearing aids	400 - 20K	1 - 1.7	63	I_Q = 0.35	up to 45
LC551	medium power hearing aids capable of driving low impedance loads	200 - 18K	1 - 1.3	48	I_Q = 0.43	up to 80*
GS551	medium power hearing aids capable of driving low impedance loads	200 - 18K	1 - 1.3	48	I_Q = 0.46	up to 80*
LC552	high gain, high power BTE and body aids	250 - 12K	1 - 1.3	75	I_Q = 0.77	up to 76

* Requires a separate preamp.

NOTE: I_A = amplifier current
I_T = transducer current
I_Q = quiescent current

PREAMPLIFIERS

PART NO.	DESCRIPTION	APPLICATION	FREQ. (Hz)	OPERATING VOLTAGE (V)	CURRENT CONSUM.(mA)	GAIN (dB)	PACKAGING
LD502	Voltage regulated, low distortion AGC compression preamp with current controlled resistance for 60 dB of gain trim.	compression amplifiers	100 - 100K	1.05 - 3	I_Q = 0.31	41	MINI 8 , PLID 8 MICRO 8
GL504	Low voltage preamp designed to drive Knowles EP receivers; MPO adjustment greater than 12 dB; low external parts count.	preamp for Knowles class D receivers	100 - 30K	1.1 - 5	I_Q = 0.15	46	PLID 8 MICRO 8
LC506	low voltage, monolithic amplifier with on-chip voltage regulator of 0.95 V.	linear preamps or low power amplifiers	200 - 5K	1.1 - 1.55	I_Q = 0.27	41	MINI 6 , PLID 8 MICRO 8
LV506	Low voltage, monolithic amplifier with on chip voltage regulator of 0.90V.	linear preamps or low power amplifiers	200 - 5K	1.1 - 1.55	I_Q = 0.27	41	MINI 6
LC507	Three transistor, class A amplifier with 20 kHz frequency response; direct replacement for OM200 and TAA141.	hearing aids, filters and micro-phone preamps	200 - 20K	1 - 3	I_Q = 1.0	76 open 58 closed	MICRO 4
LX509	Four inverting preamps, one of which has 6 dB greater drive current.	active filters, multi-channel aids and telecoil preamps	unity gain BW ~150K	1 - 5	I_Q = 0.21	56 open 30 closed	PLID 10 MICRO 10

PROGRAMMABLE SERIES

PART NO.	DESCRIPTION	APPLICATION	SUPPLY VOLTAGE (V)	QUIESCENT CURRENT (mA)	PACKAGING
GP520	Programmable analog signal path; gain, high cut, low cut, AGC threshold, release time, MPO and receiver current are programmable; designed to be controlled by the GP521 memory unit; class A output stage.	programmable hearing aids; master hearing aid	1.3	I_Q = 0.5	Due to the large number of pins in the circuit, this product is available in chip or hybrid form only.
GP521	General purpose EEPROM non-volatile CMOS memory/controller; 8 programmable current sinks (PCS) with option to configure to 4 regular PCS outputs and 2 switchable PCS outputs; temporary RAM; single battery voltage compatible; 50 kHz max. clock rate	programmable hearing aids; memory unit	1.3	I_Q = 0.25	Due to the large number of pins in the circuit, this product is available in chip or hybrid form only.
Interface Module	TTL to 1.3V logic converter, 1.3V regulator, low voltage indicator, thermal shutdown circuitry	programmable hearing aid interface for GP521	N/A	N/A	25 pin D-shell connector, plugs into parallel printer port

SPECIAL CIRCUITS

LV560	Low voltage, digitally controlled transconductance block with memory; typical impedances ranging from 4 kΩ to 500 kΩ in 2.5 dB steps; ground referenced switch.	electronic volume control; attenuators; digitally controlled impedances	1 - 5	I_Q = 0.076	PLID 10, MICRO 10,
GT560	Low voltage, digitally controlled transconductance block with memory; supply referenced switch; touch plate compatibility (30 MΩ); mid-gain power-up setting.	electronic volume control; attenuators; digitally controlled impedances	1 - 5	I_Q = 0.076	PLID 10, MICRO 10
LF580	Two single 12 dB/oct or one 24 dB/oct analog highpass Butterworth filter; 200 to10 kHz adjustable corner frequency; low external parts count; unity gain.	active tone control	1.1 - 3	I_Q = 0.28	MINI 8, PLID 8 MICRO 8
LF581	12 dB/oct unity gain highpass Butterworth filter; 200 to 2 kHz adaptive cut-off frequency; capable of sensing long term average noise and reducing low frequency noise by shifting the corner frequency; 20 dB increase in the input results in an increase in the cut-off frequency.	active tone control; automatic highpass filtering; hearing aid low frequency noise reduction	1.1 - 3	I_Q = 0.26	PLID 10, MICRO 10
LS581	12 dB/oct unity gain highpass filter; adaptive cut-off frequency; 20 dB increase in the input results in an increase in the cut-off frequency; on-chip preamp.	active tone control; automatic highpass filtering; hearing aid low frequency noise reduction	1.1 - 3	I_Q = 0.30	PLID 10, MICRO 10